Intel (R) Pentium (R) III Processor / 840 Development Board Schematics

REV B
2000

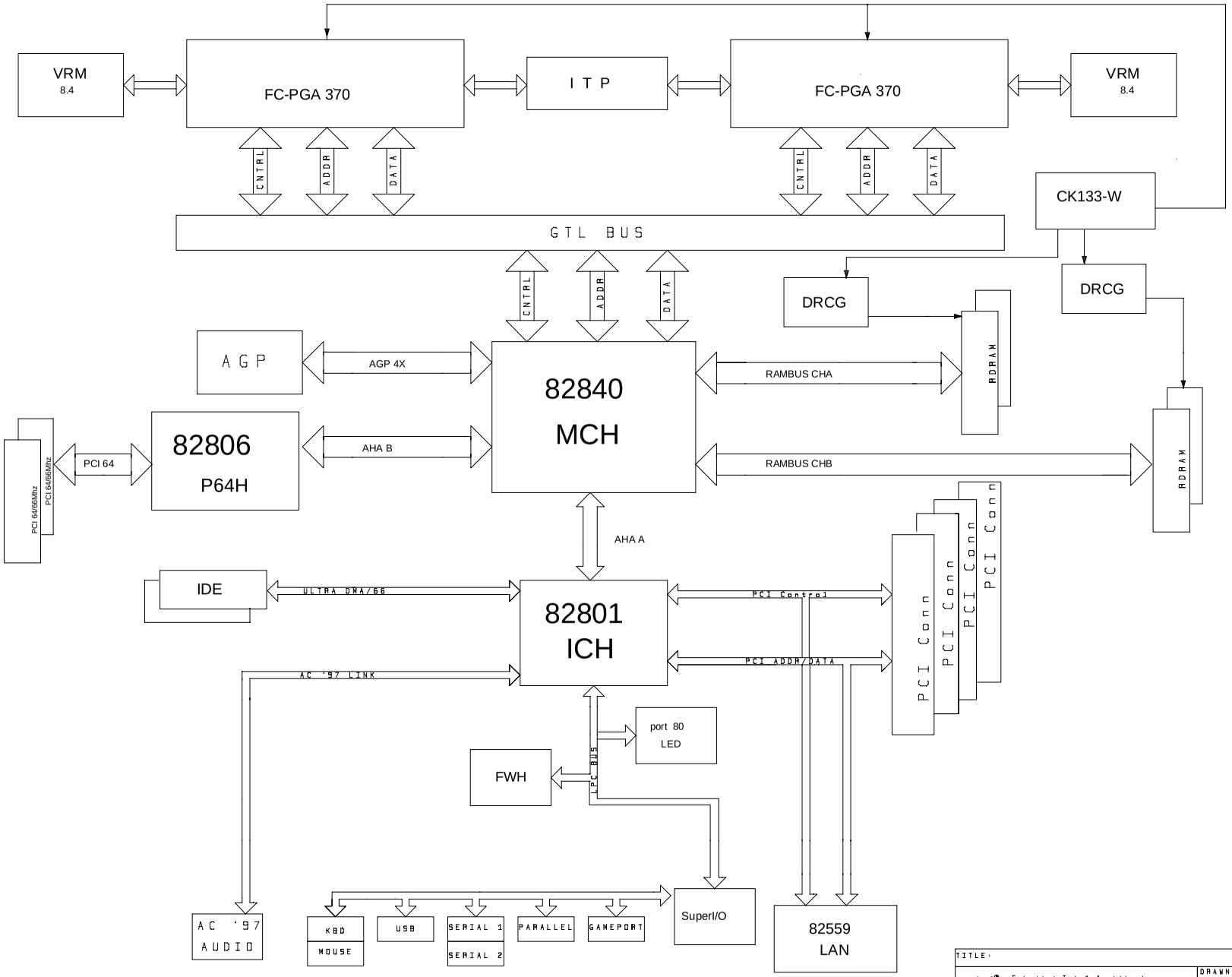
Contents

Revision History

Rev A - Initial release
Rev B - Change ITP to work with American Arium
Change PSB ECC enable

GTLREFA = 2/3 * 1.5V = 1.125V
GTLREFB = 2/3 * 1.5V = 1.125V
HUBREF_ICH= 1/2 * 1.8V = 0.9V
HUBREF_MCH= 1/2 * 1.8V = 0.9V
HUBREF_P64H= 2/3 * 1.8V = 1.35V
CHA_R_VREF= 0.777* 1.8V = 1.4V
CHB_R_VREF=0.777 * 1.8V = 1.4V

TITLE:		Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 4-13-2000_11:59	1 OF 53


VRM
8.4
FC-PGA 370
I T P
FC-PGA 370
VRM
8.4
CNTRL
ADDR
DATA
CNTRL
ADDR
DATA
CK133-W
GTL BUS
CNTRL
ADDR
DATA
DRCG
DRCG
RDRAM
A G P
AGP 4X
82840
MCH
RAMBUS CHA
RDRAM
PCI 64/66Mhz
PCI 64/66Mhz
PCI 64
82806
P64H
AHA B
RAMBUS CHB
AHA A
IDE
ULTRA DMA/66
82801
ICH
PCI Control
PCI ADDR/DATA
PCI Conn
PCI Conn
PCI Conn
PCI Conn
AC '97 LINK
port 80
LED
FWH
LPC BUS
AC '97
AUDIO
KBD
MOUSE
USB
SERIAL 1
SERIAL 2
PARALLEL
GAMEPORT
SuperI/O
82559
LAN
TITLE:
Rev: A
Embedded Intel Architecture
DRAWN BY:
TL
PROJECT:
LAST REVISED:
3-8-2000 16:47
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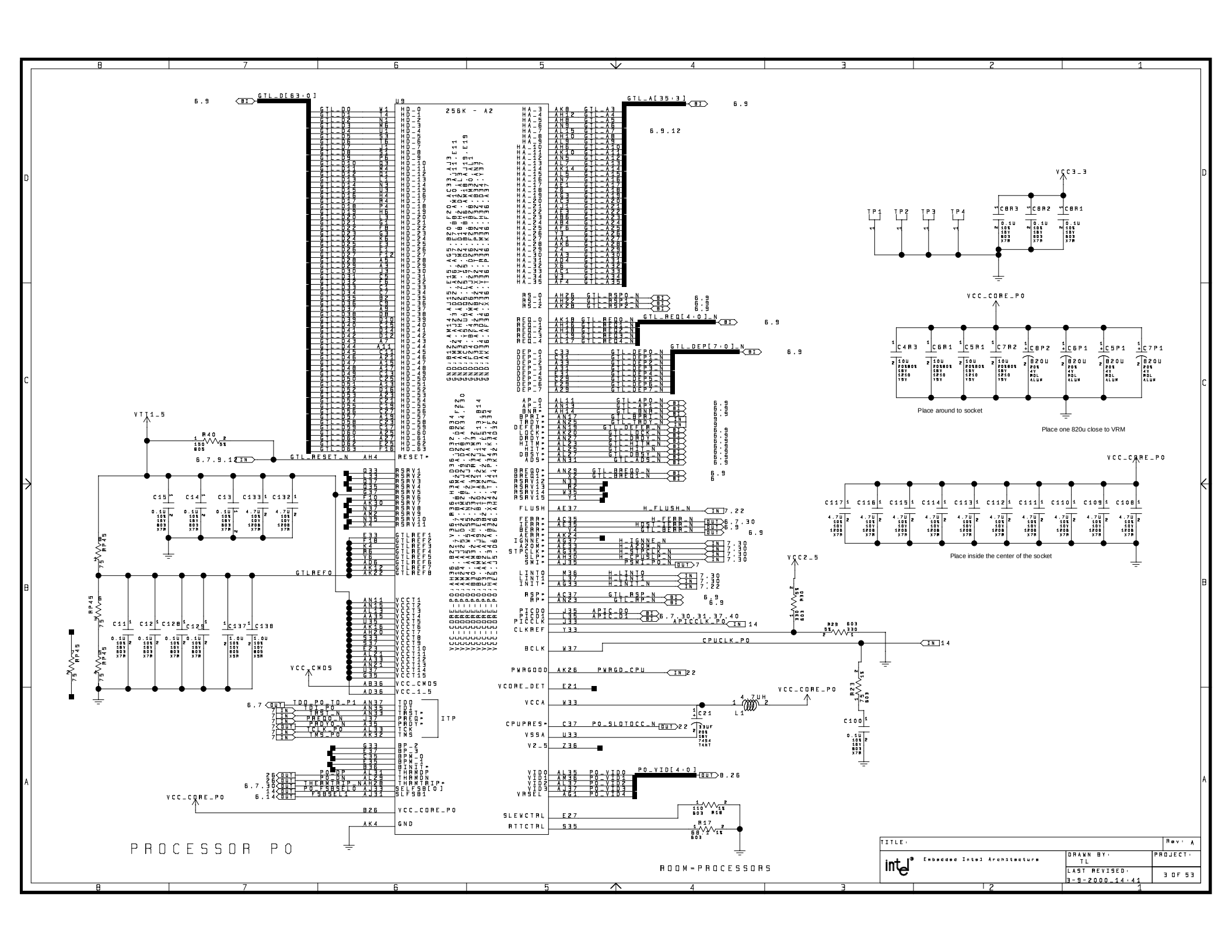
PROCESSOR PO
ROOM=PROCESSORS
Place around to socket
Place one 820u close to VRM
Place inside the center of the socket
TITLE:
Rev: A
Embedded Intel Architecture
DRAWN BY: TL
PROJECT:
LAST REVISED: 3-9-2000 14:41
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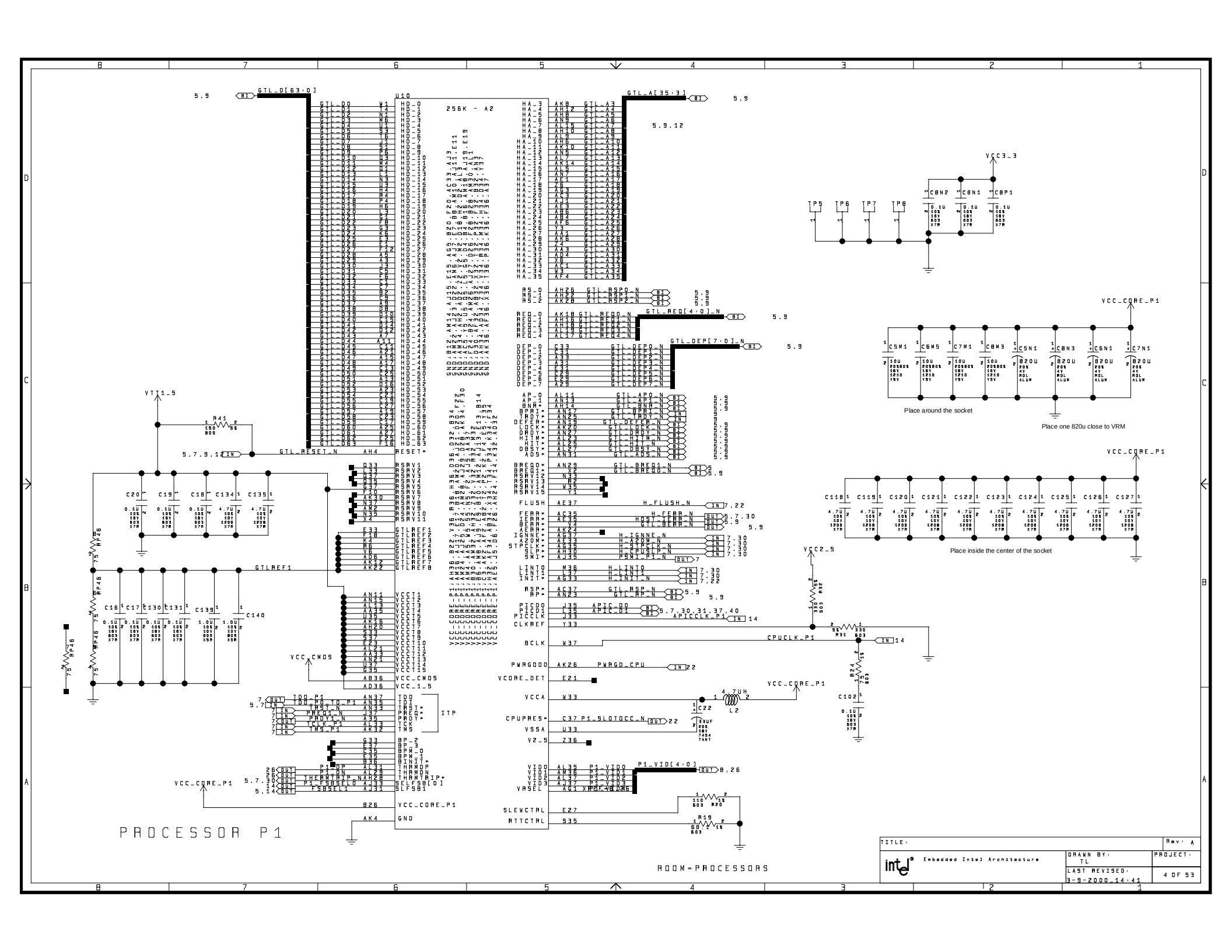
PROCESSOR P1
U10
256K - A2
GTL_D[63:0]
GTL_A[35:3]
GTL_REQ[4:0]_N
GTL_DEP[7:0]_N
GTL_RESET_N
VCC_CORE_P1
VCC_CMOS
VCC2_5
VCC3_3
VTT1_5
CPUCLK_P1
PWRGD_CPU
P1_VID[4:0]
ITP
Place around the socket
Place one 820u close to VRM
Place inside the center of the socket
ROOM=PROCESSORS
TITLE:
Rev: A
intel
Embedded Intel Architecture
DRAWN BY: TL
PROJECT:
LAST REVISED: 3-9-2000 14:41
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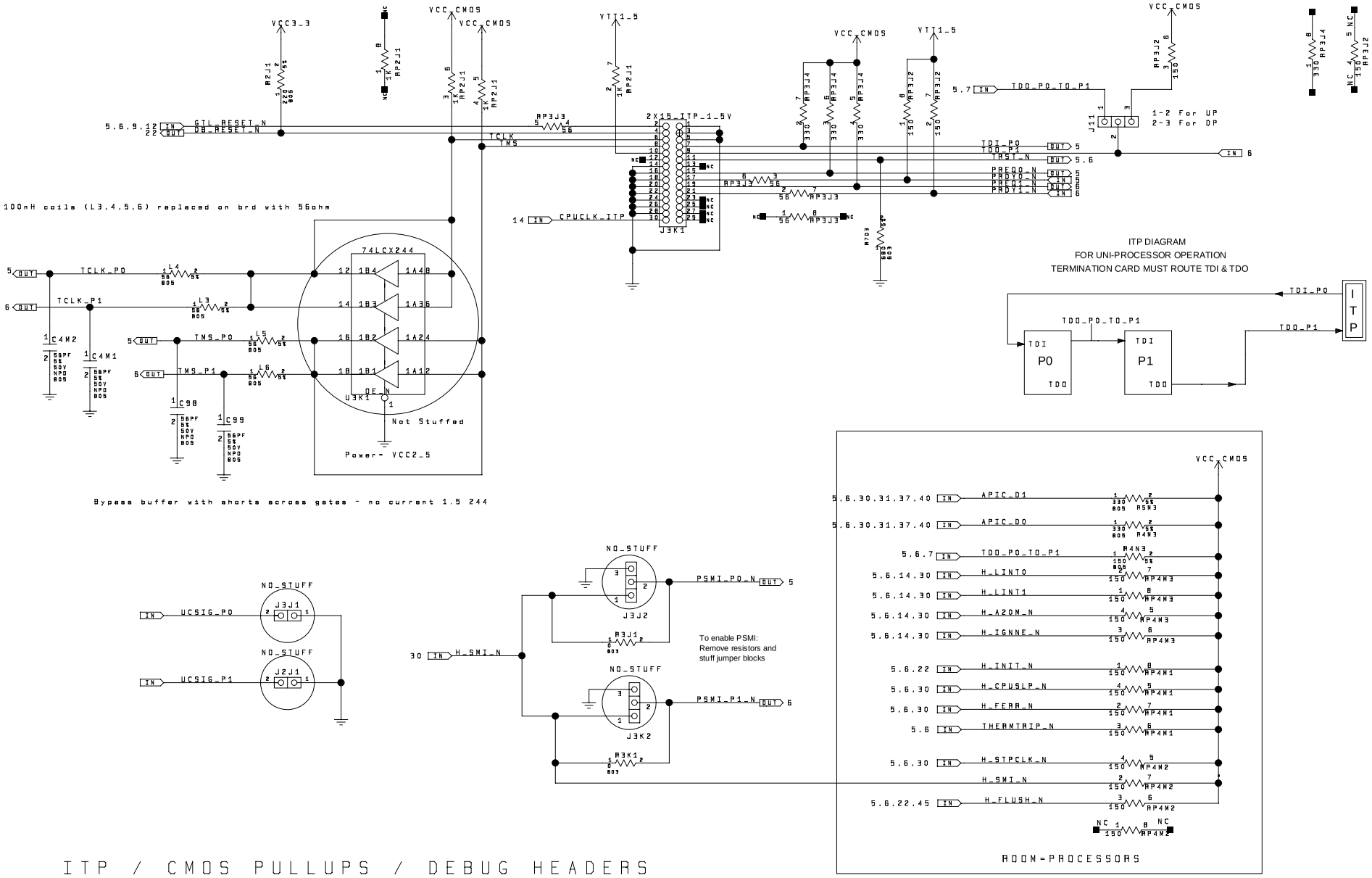
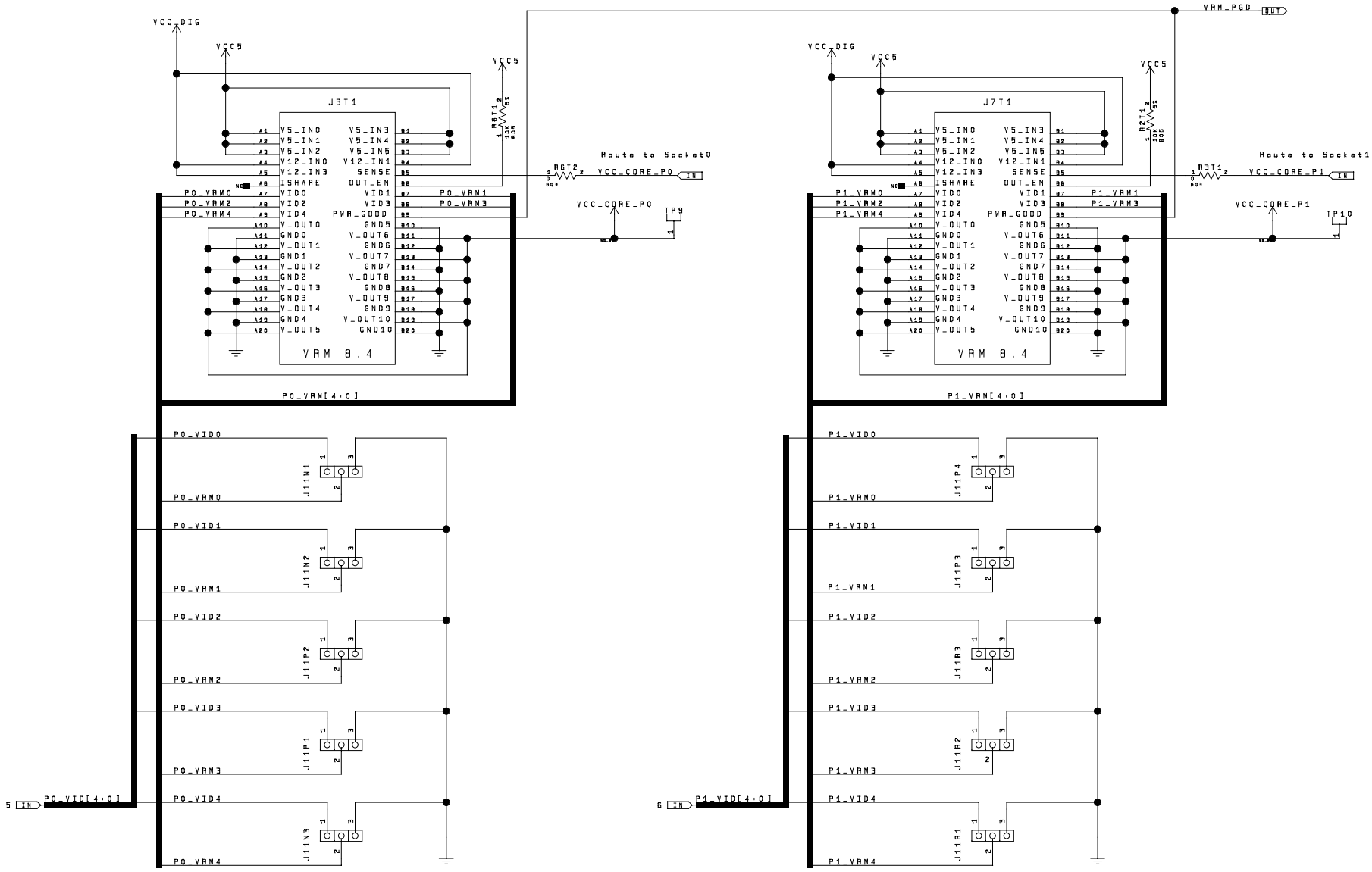


ITP / CMOS PULLUPS / DEBUG HEADERS

TITLE:		Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 4-14-2000 8:28	5 OF 53



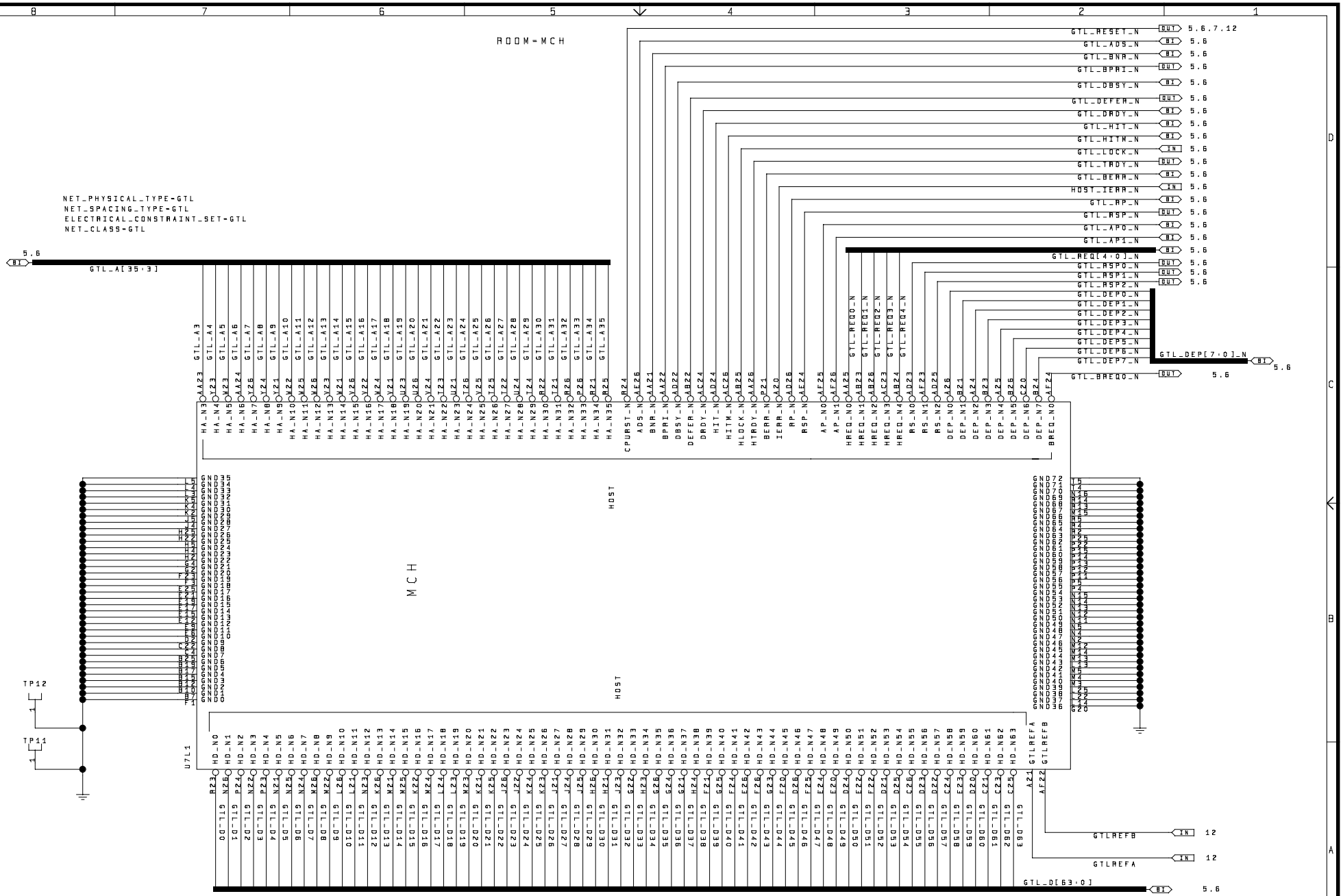
VID4 Must be grounded for production FC_PGA

Jumper position	1-2	2-3	No jumper
VRM VID[4:0]	CPU VID[4:0]	0	1

VRM HEADERS FOR PROCESSOR SOCKETS

ROOM=VRM

TITLE:		Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 3-9-2000 14:41	6 OF 53



82840 MCH PSB SIGNALS

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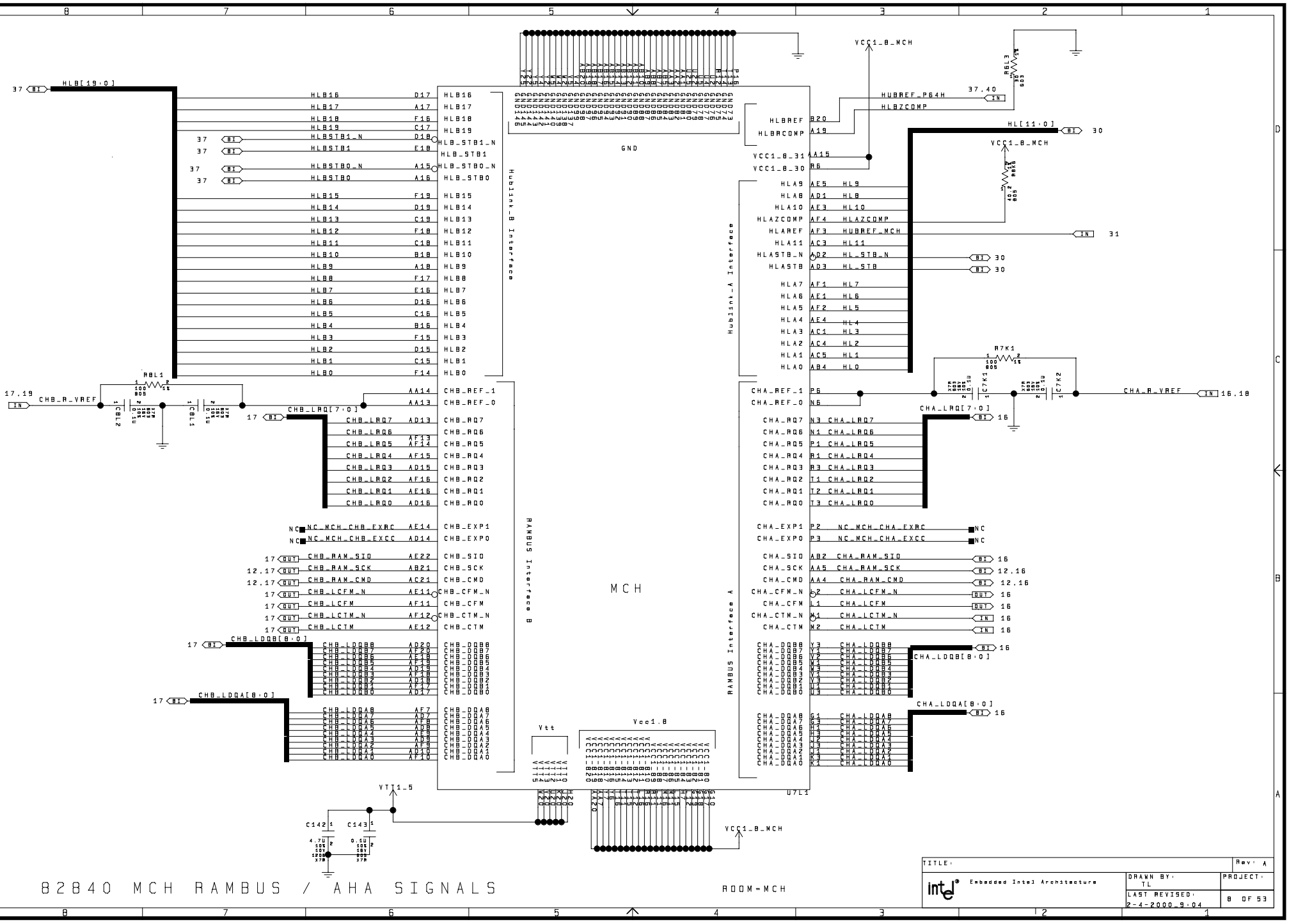
intel Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
LAST REVISED: 2-4-2000 9:03	7 OF 53



82840 MCH RAMBUS / AHA SIGNALS

ROOM=MCH

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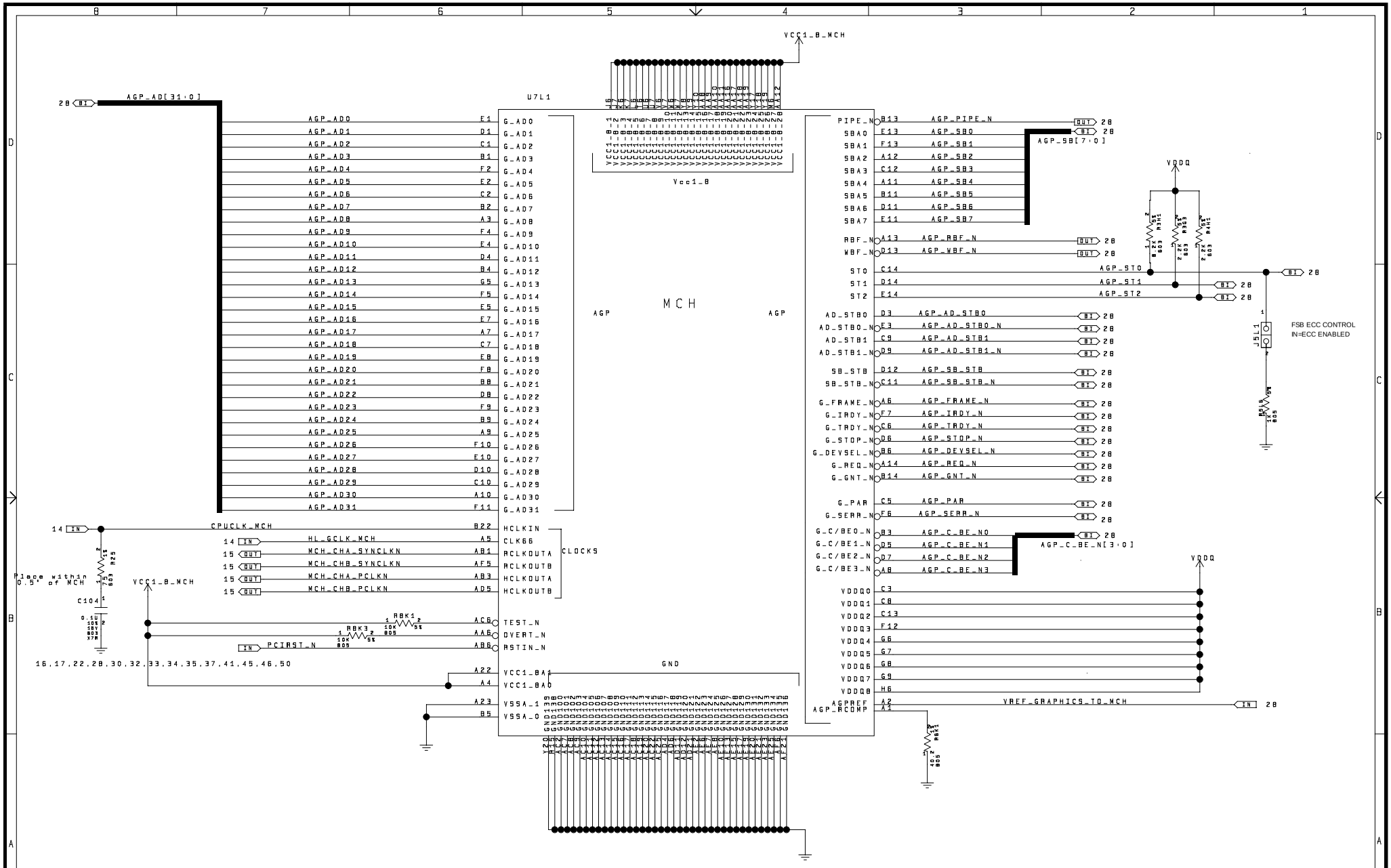
intel Embedded Intel Architecture	PROJECT:
DRAWN BY: TL	
LAST REVISED: 2-4-2000 9:04	8 OF 53



82840 MCH AGP SIGNALS

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intel Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
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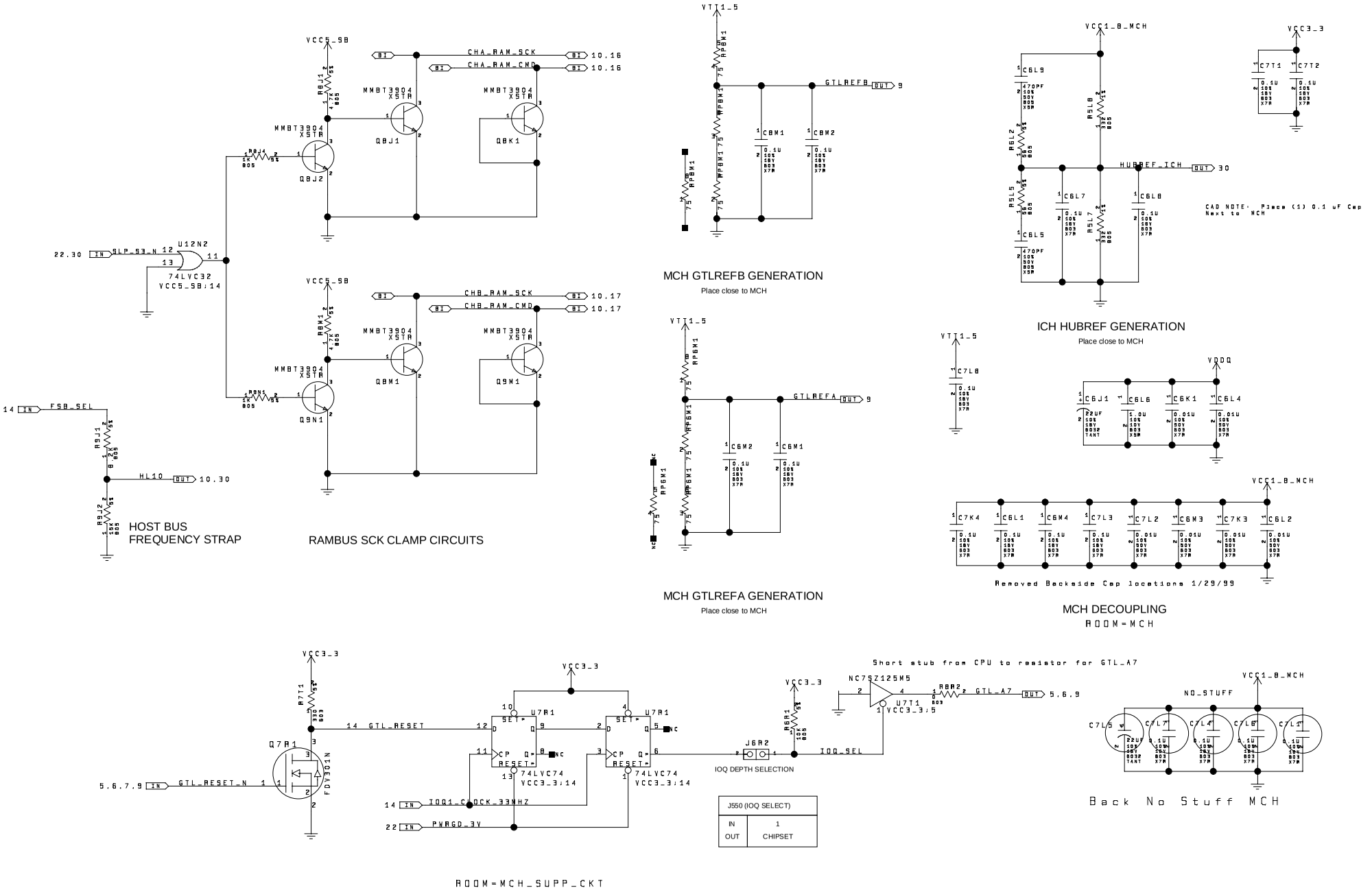

82840 MCH DECOUPLING AND SUPPORT CIRCUITRY

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intel® Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
	LAST REVISED: 2-4-2000 9:05
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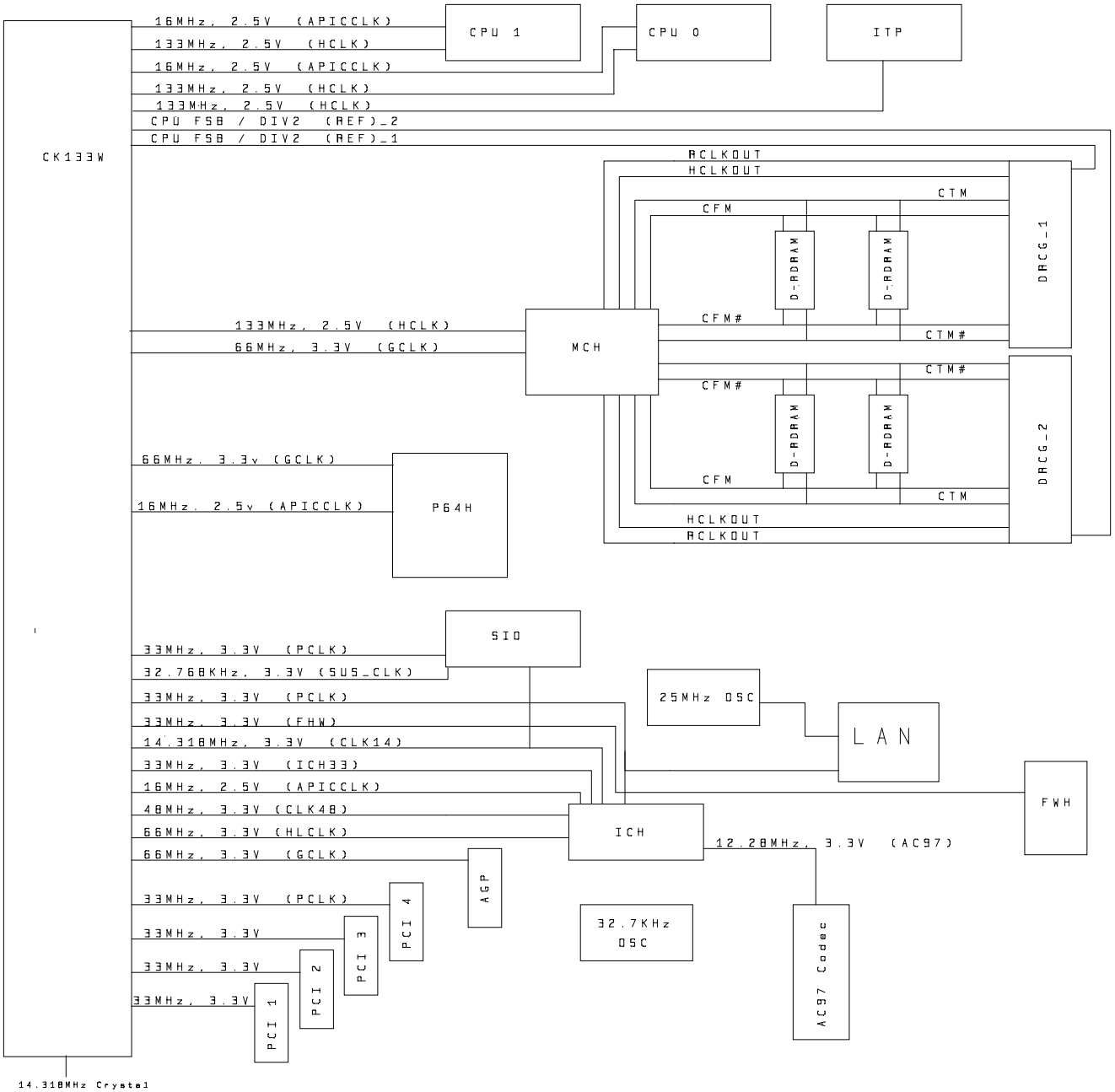

CLOCK DISTRIBUTION

NOTES:

HCLK: 100 Processor & MCH FSB
GCLK: 66MHz, AGP, AHA, P64H
CTM/CFM: 300MHz, RDRAM-D, MCH RAC
APICCLK: 16.67MHz, APIC BUS
PCLK: 33MHz, PCI Bus & LPC Bus
CLK48: 48MHz, USB & SIO
CLK14: 14.318MHz, 8254 Timers
RTC: 32.768MHz, ICH
OSC: 14.318, ICH (ACPI Timer)
AC97: 12.288MHz, AC97 Audio Codec
ICH33: 33MHz, ICH (Free Running PCI)

2-4-2000_9:06

TITLE:		Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
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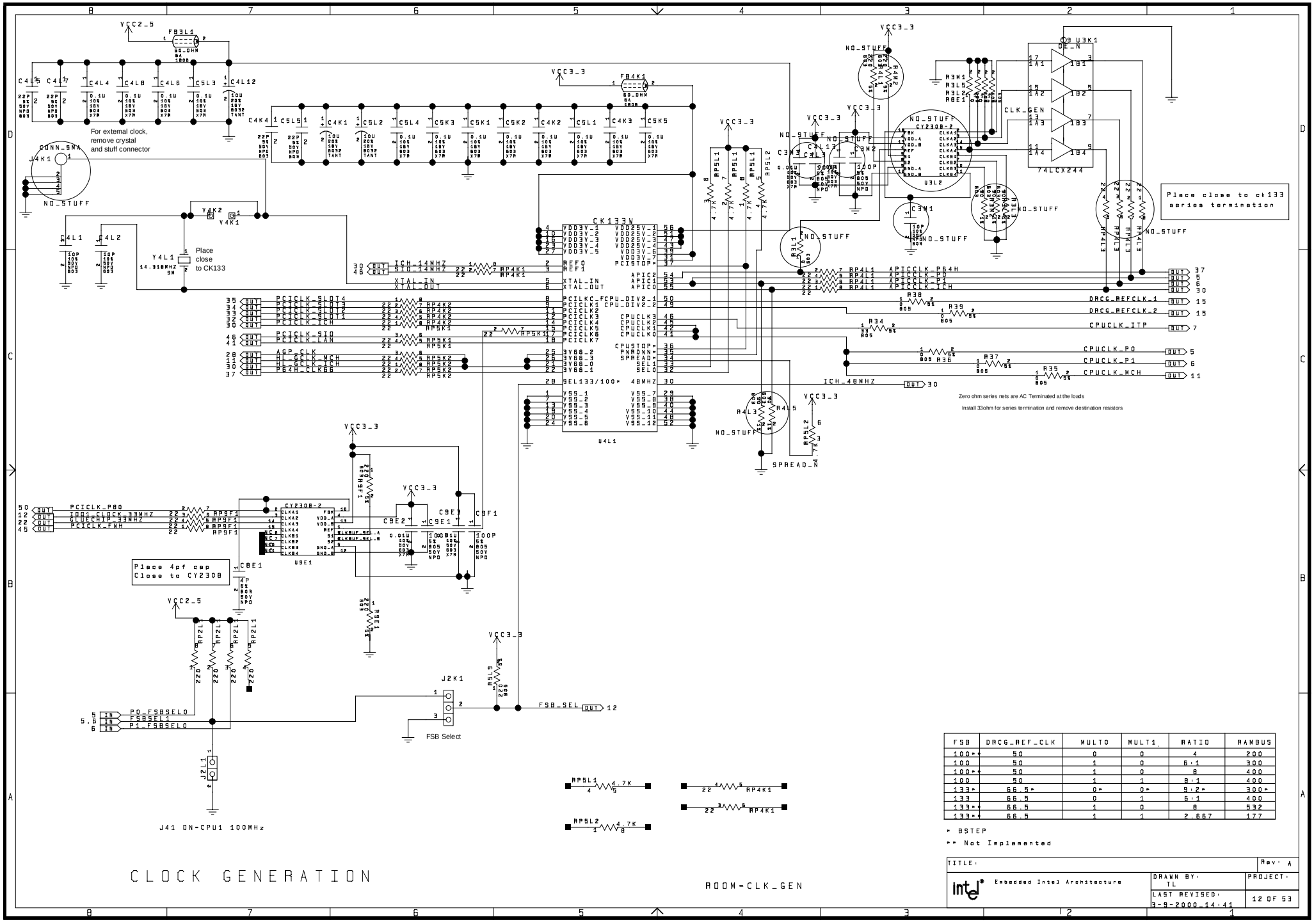

FSB	DRCG_REF_CLK	MULT0	MULT1	RATIO	RAMBUS
100**	50	0	0	4	200
100	50	1	0	6:1	300
100**	50	1	0	8	400
100	50	1	1	8:1	400
133*	66.5*	0*	0*	9:2*	300*
133	66.5	0	1	6:1	400
133**	66.5	1	0	8	532
133**	66.5	1	1	2.667	177

* BSTEP

** Not Implemented

TITLE:	Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
	LAST REVISED: 3-9-2000.14:41
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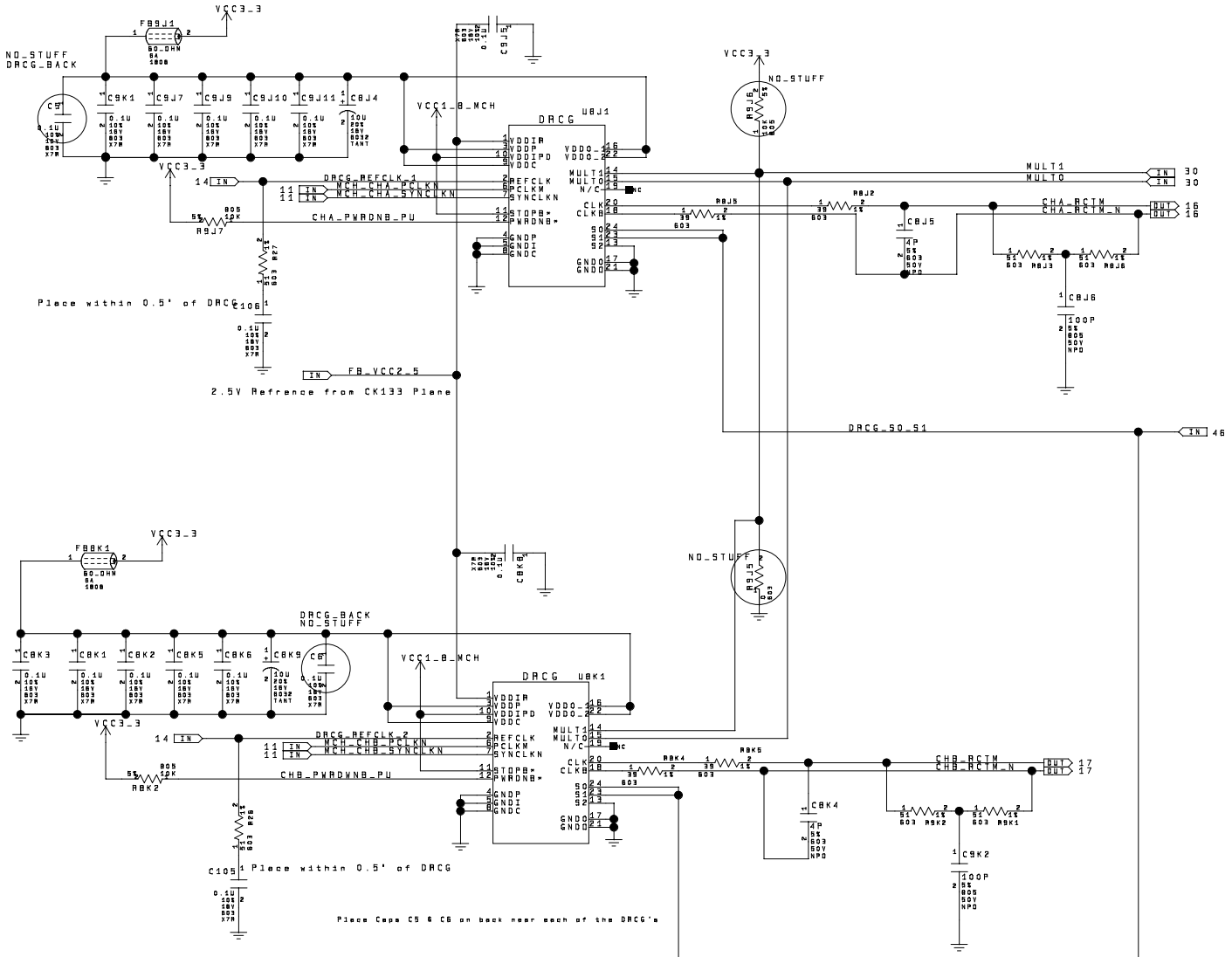

RAMBUS FREQUENCY SELECTION

FSB	DRCG_REF_CLK	MULT0	MULT1	RATIO	RAMBUS
100**	50	0	0	4	200
100	50	0	1	6	300
100**	50	1	0	8	400
100	50	1	1	8:1	400
133*	66.5	0	0	9:2	300
133	66.5	0	1	6	400
133**	66.5	1	0	8	532
133**	66.5	1	1	2.667	177

* BSTEP
** Not Implemented

RAMBUS DRCG MODE CONTROL

S0	S1	MODE
0	0	Normal
0	1	Output Enable Test
1	0	Bypass
1	1	Test

In Test Mode, Refclk is passed to the outputs

DRCG

ROOM=DRCG

TITLE:	Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL
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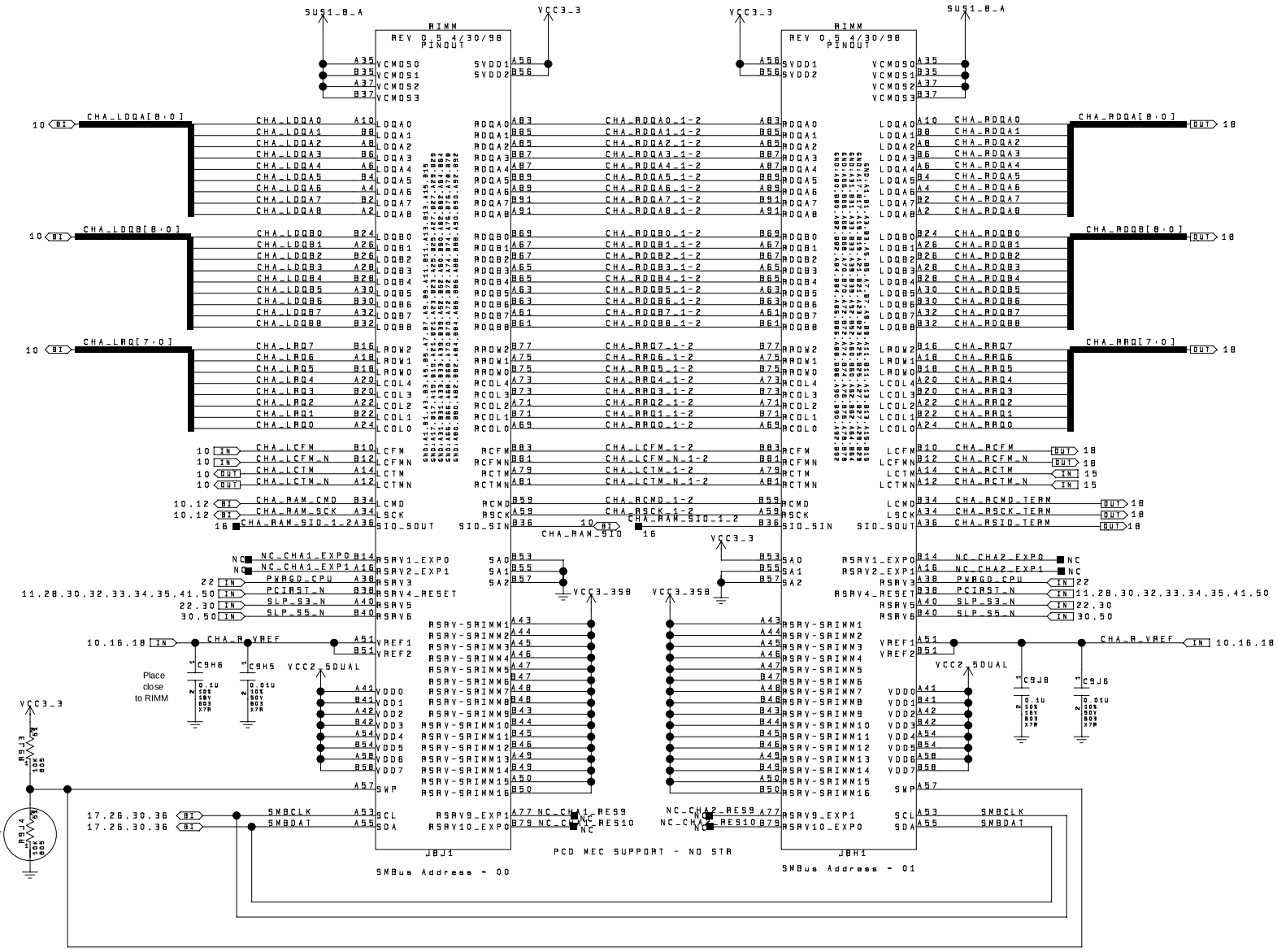

RIMM CHA CONNECTORS

ROOM=RIMM_CHA

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intel® Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
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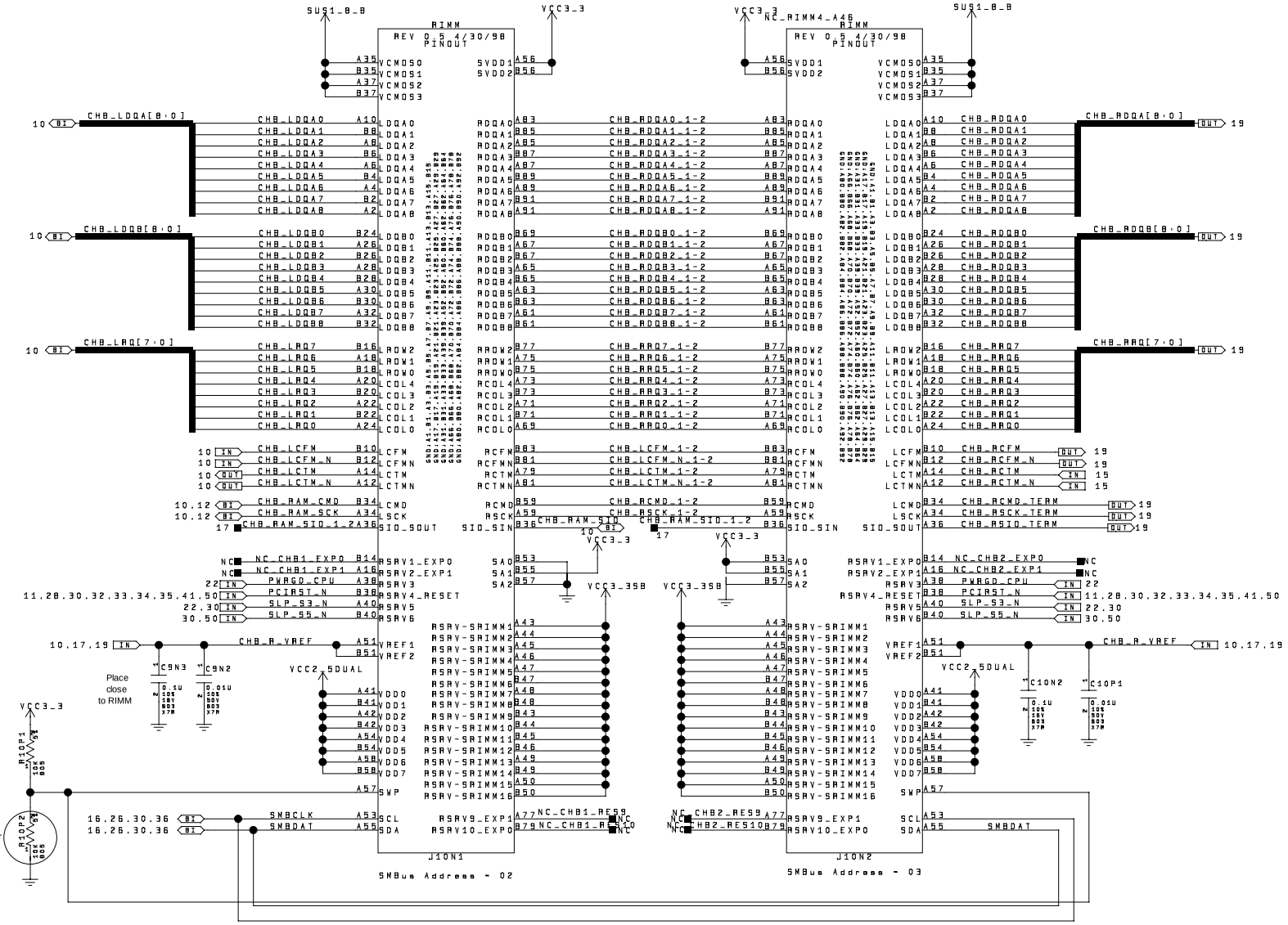

RIMM CHB CONNECTORS

ROOM=RIMM_CHB

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intel® Embedded Intel Architecture	DRAWN BY: TL
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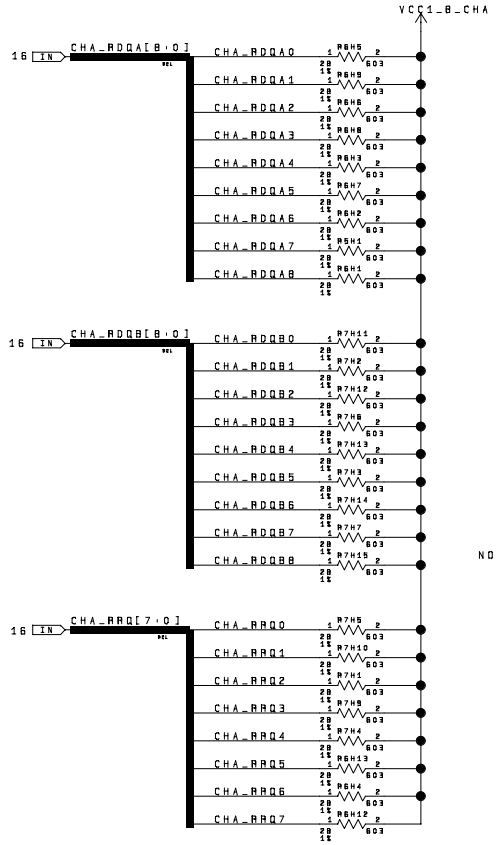
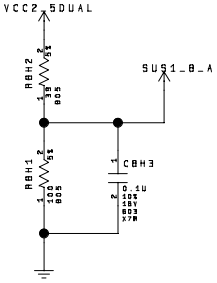
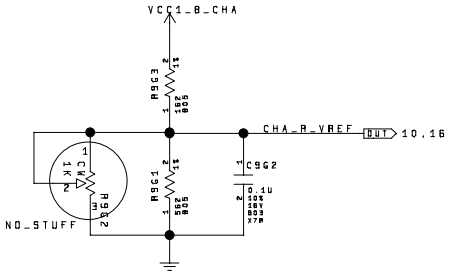
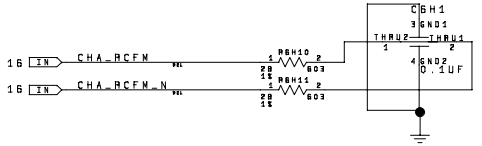


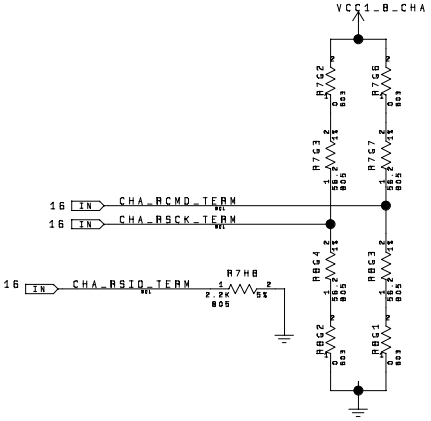


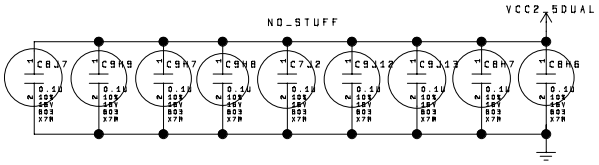
RAMBUS SUS1.8V GENERATION



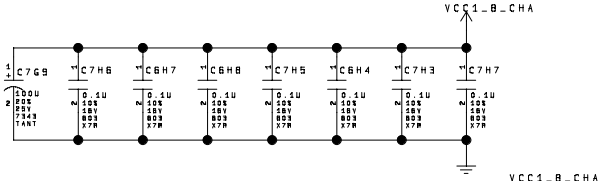
RAMBUS VREF GENERATION

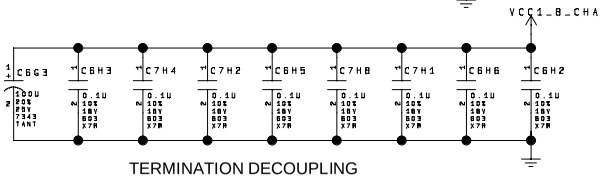






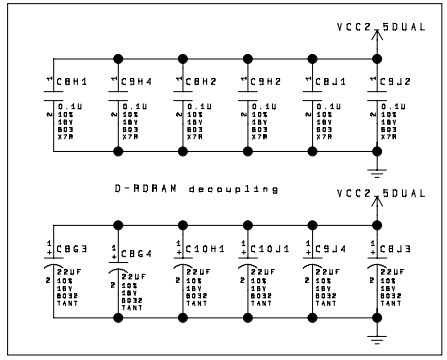
Back No Stuff Decouple

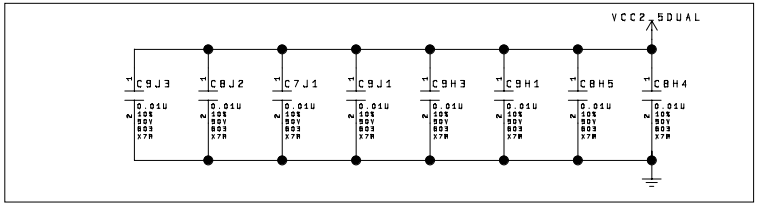




TERMINATION DECOUPLING
(one 0.1uF cap per 2 RSL lines)

Vias for RSL test traces





RIMM DECOUPLING

ROOM=RIMM_CHA

RDRAM CHA TERMINATION AND DECOUPLING

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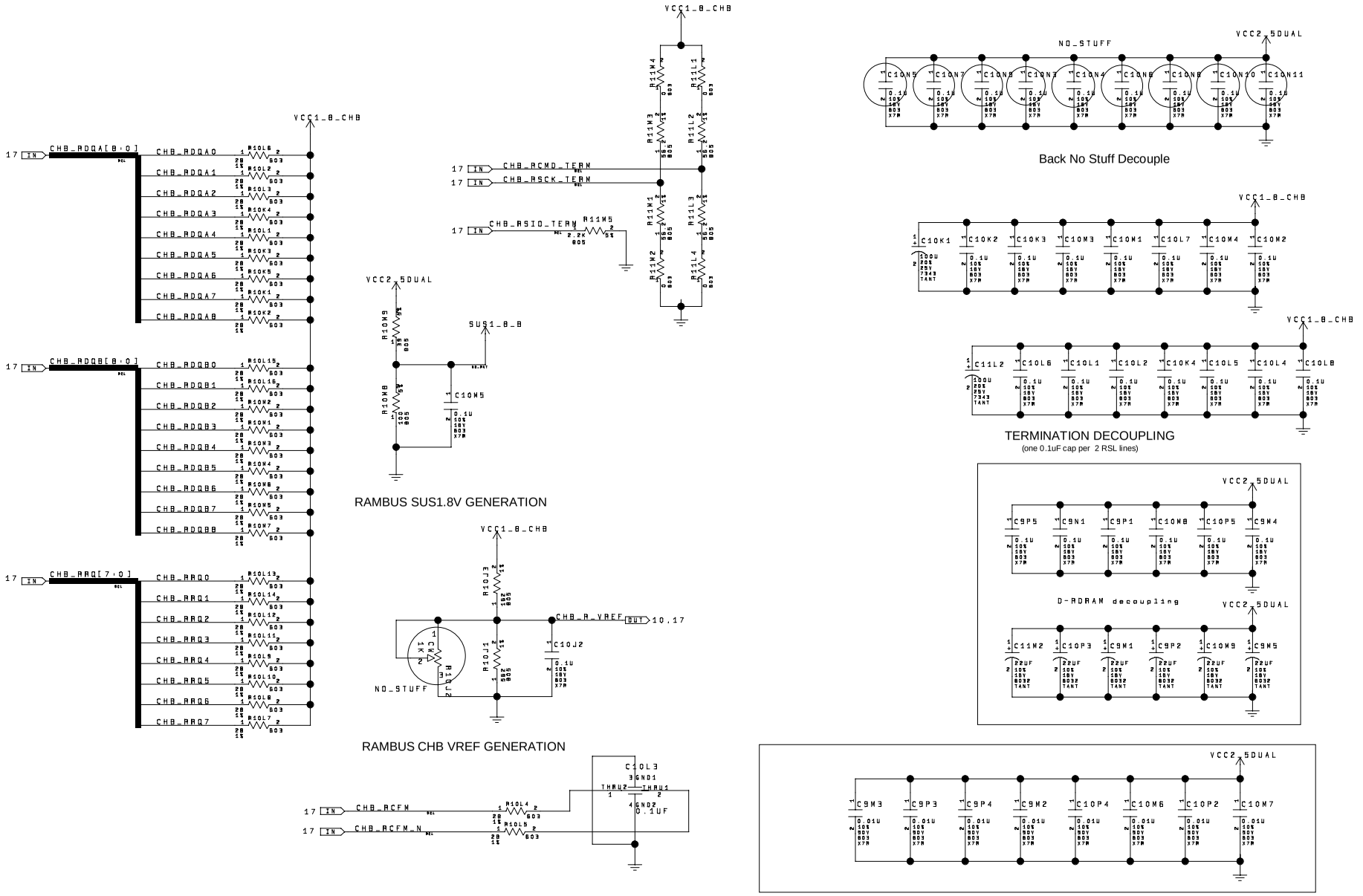

RDRAM CHB TERMINATION AND DECOUPLING

TITLE:	Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
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WTX POWER SUPPLY

VCC3_3SB

82559 LOM
SRIMMs
ADM1024
ICH, SIO
PCI32,PCI64, AMR

p.22

VCC5

CPUs,
VRMs,
AGP, PCI32, PCI64
AMR, Port 80,
USB, KBD/MS

VCC5_SB

WAKE ON LAN
COM1

VCC12

VRMs, FANs,
AGP, PCI32, AMR,
MIC AMP,PCI64
COM PORTs

VCC_DIG

VRM P0
VRM P1
RAMBUS ISR 2.5V

p.22

VCC3_3

CPUs,
CK133,
DRCG,
RIMMs,
AGP,ICH,
FWH,SIO,P64H
PCI32, PCI64, AMR
GAMEPORT

VCC-12

PCI32, PCI64, AMR
MIC AMP,
COM PORTs

VOLTAGE REGULATORS

VTT1_5

CPUs

p.21

AGP1_5

AGP

p.21

VCC1_8

ICH, P64H

p.21

VCC1_8_MCH

MCH
DRCG

p.21

VCC2_5DUAL

RIMMs

p.22

VCC2_5

CK133
DRCG
ITP CLK BUFFER

p.22

VCC_CMOS

CMOS PULLUPS

2.5V

p.22

AUDVCC5

AD1881 AUDIO
LM4880 AMP

p.38

SUS1_8A

RIMMs

p.16

SUS1_8B

RIMMs

p.17

VCC1_8_CHA
VCC1_8_CHB

RIMM TERM

p.17

VRMs

VCC_CORE_P0

CPU0

p.9

VCC_CORE_P1

CPU1

p.9

SWITCHED VOLTAGE PLANES

VDDQ

VCC3_3 / AGP1_5

AGP
MCH

p.25

Note: Only major devices are listed in this diagram

POWER MANAGEMENT MAP

TITLE:		Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
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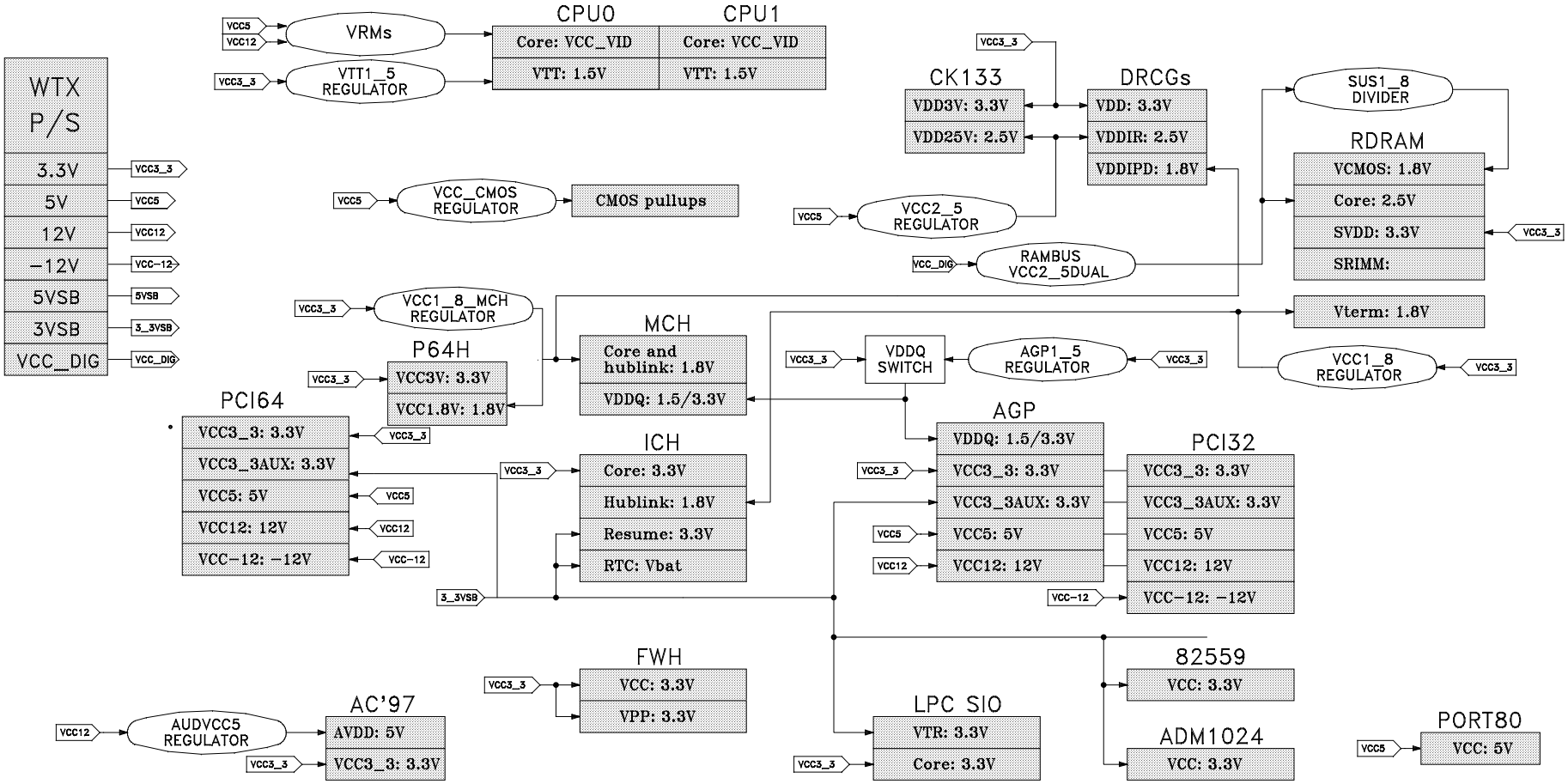

AHA: Vdd = 1.8V, Vref = 0.5 Vdd
RSL: Vtt=1.8V, Vref = 2/3 Vtt
GTL: Vtt=1.5V, Vref = 2/3 Vtt
AGP: Vdd= 1.5V or 3.3V, Vref= 0.5 Vagpdd (1.5V) or 0.4 Vagpdd (3.3V)

POWER DISTRIBUTION MAP

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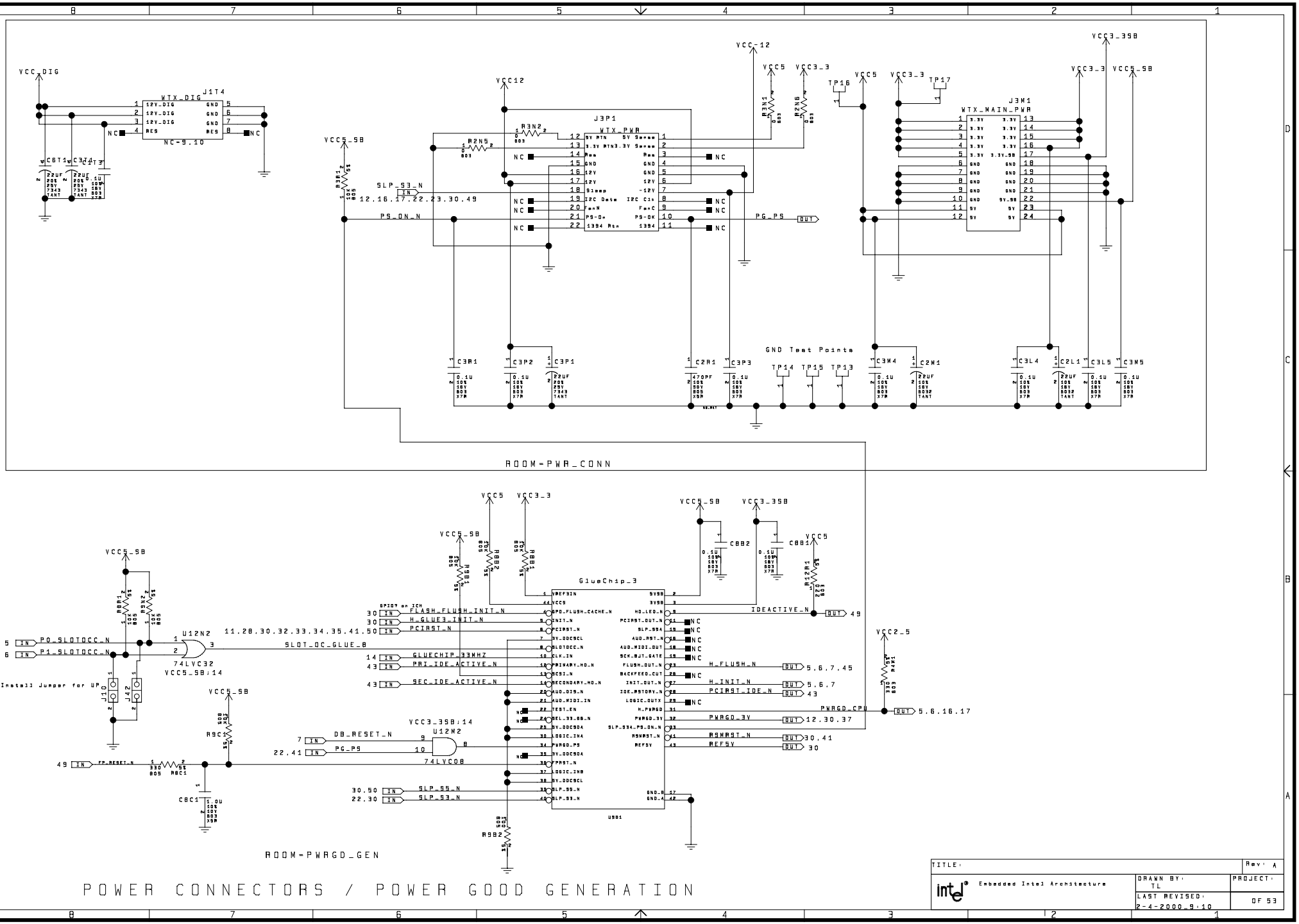
intel Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 3-8-2000 16:50	19 OF 53


VCC_DIG
J1T4
WTX_DIG
12V_DIG
GND
RES
NC
NC-9.10
C8T1
C3T4
C4T1
22UF
0.1U
VCC12
VCC5
VCC3_3
VCC3_3SB
VCC5_SB
J3P1
WTX_PWR
5V MTN
5V Sense
3.3V MTN
3.3V Sense
Res
Fan
12V
-12V
Sleep
I2C Data
I2C Clk
PS-On
PS-OK
1394
1394 Res
R3N2
R2N5
R3R1
R3N1
R2N6
SLP_S3_N
12,16,17,22,23,30,49
PS_ON_N
PG_PS
OUT
J3M1
WTX_MAIN_PWR
3.3V
3.3V_SB
5V_SB
TP16
TP17
C3R1
C3P2
C3P1
C2R1
C3P3
C3M4
C2M1
C3L4
C2L1
C3L5
C3M5
GND Test Points
TP14
TP15
TP13
ROOM=PWR_CONN
U12N2
74LVC32
VCC5_SB;14
P0_SLOTOCC_N
P1_SLOTOCC_N
11,28,30,32,33,34,35,41,50
SLOT_OC_GLUE_B
Install Jumper for WP
J1J0
J4J2
R9C1
C8C1
U12M2
74LVC08
VCC3_3SB;14
DB_RESET_N
PG_PS
FP_RESET_N
GlueChip_3
U9B1
FLASH_FLUSH_INIT_N
H_GLUE3_INIT_N
PCIRST_N
GLUECHIP_33MHZ
PRI_IDE_ACTIVE_N
SEC_IDE_ACTIVE_N
SLP_S5_N
SLP_S3_N
30,50
22,30
R9B2
R9B1
R9B3
C8B2
C8B1
R12R1
IDEACTIVE_N
H_FLUSH_N
H_INIT_N
PCIRST_IDE_N
PWRGD_CPU
PWRGD_3V
RSMRST_N
REF5V
VCC2_5
R9M1
ROOM=PWRGD_GEN
POWER CONNECTORS / POWER GOOD GENERATION
TITLE:
Rev: A
intel
Embedded Intel Architecture
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LAST REVISED: 2-4-2000 9:10
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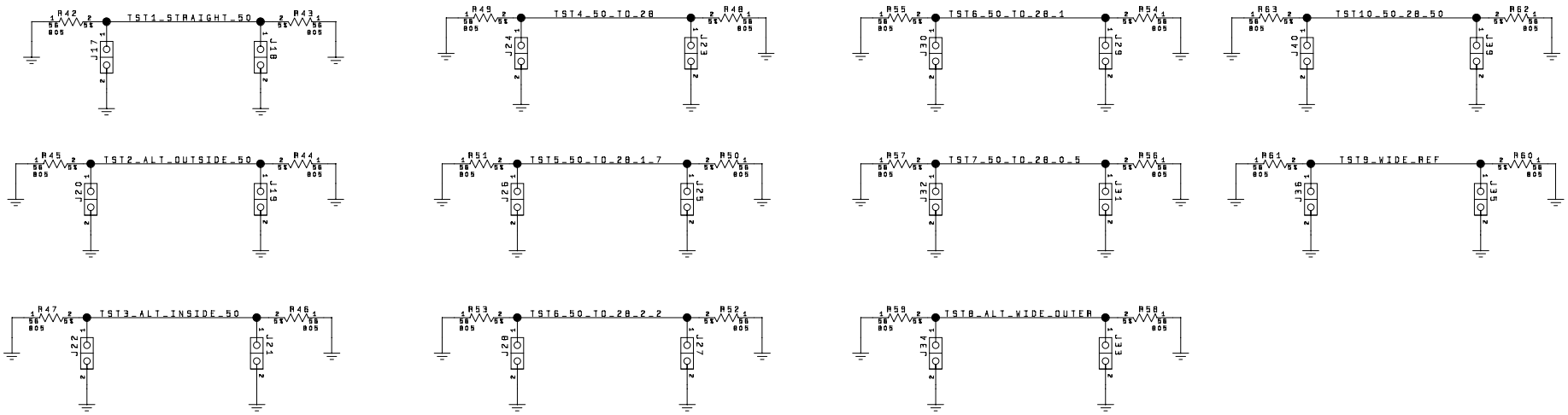
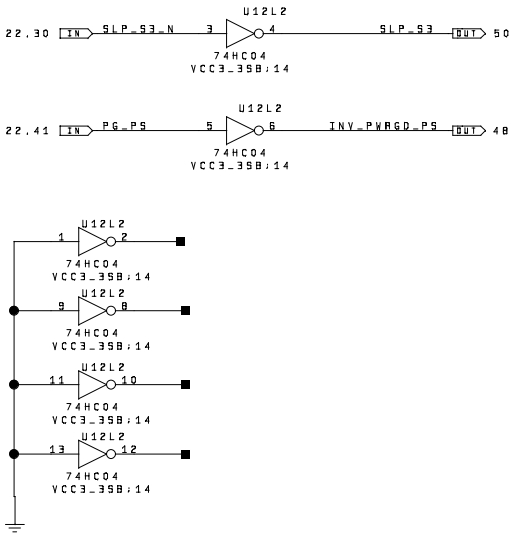


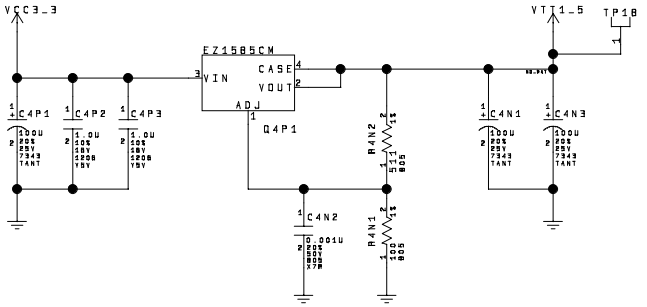
Impeadance Test Traces



POWER MANAGEMENT LOGIC

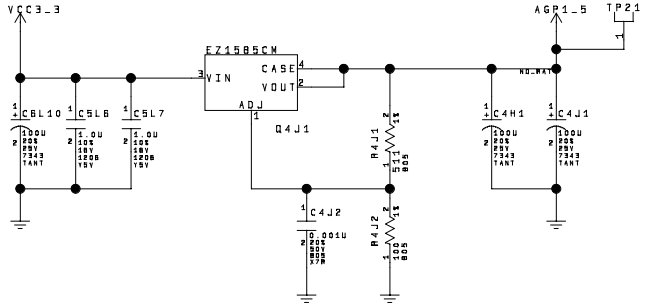
ROOM=PWR_MGMT_LOGIC

TITLE:		Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 2-4-2000_9:14	21 OF 53



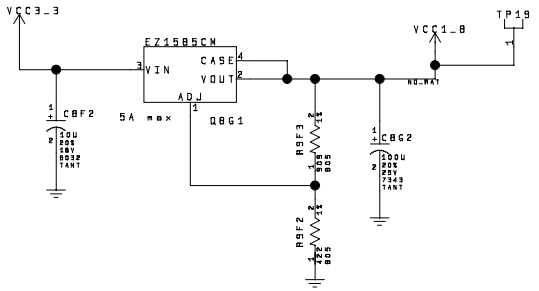
VTT 1.5V GENERATION

ROOM=VTT_1.5V_GEN



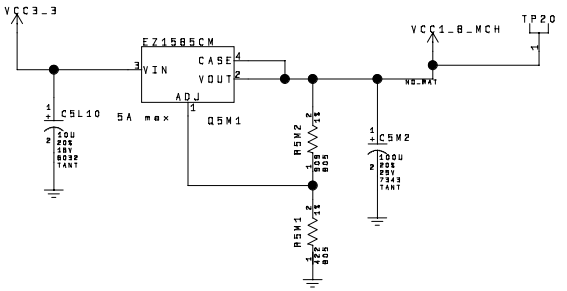
AGP 1.5V GENERATION

ROOM=AGP_1.5V_GEN



1.8V GENERATION

ROOM=1.8V_GEN

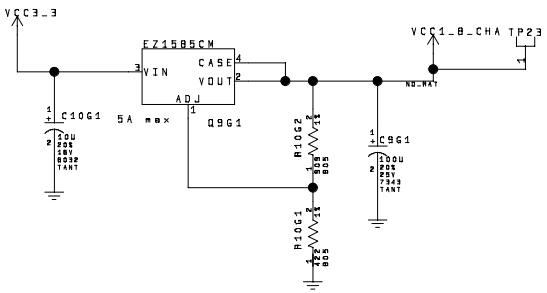


MCH 1.8V GENERATION

ROOM=MCH_1.8V_GEN

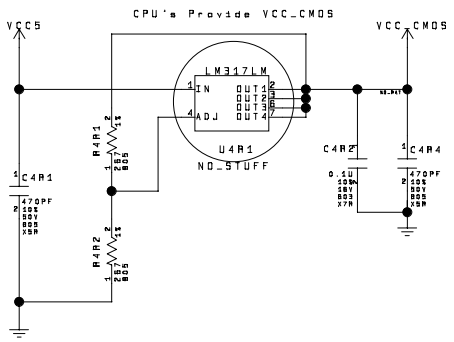
1.5V / 1.8V REGULATORS

TITLE:		Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 2-4-2000 9:14	22 OF 53



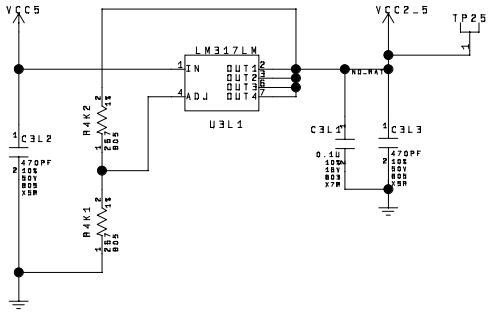
1.8V GENERATION FOR RAMBUS CHA TERM

ROOM=1.8V_GEN



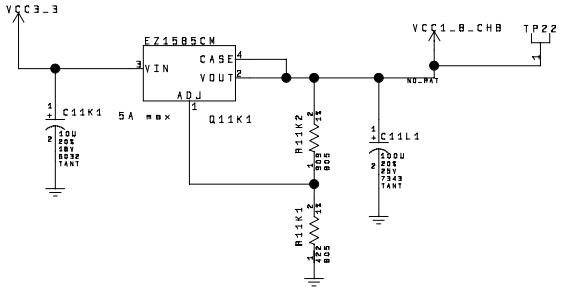
FSB CMOS VOLTAGE GENERATION

ROOM=FSB_CMOSV_GEN



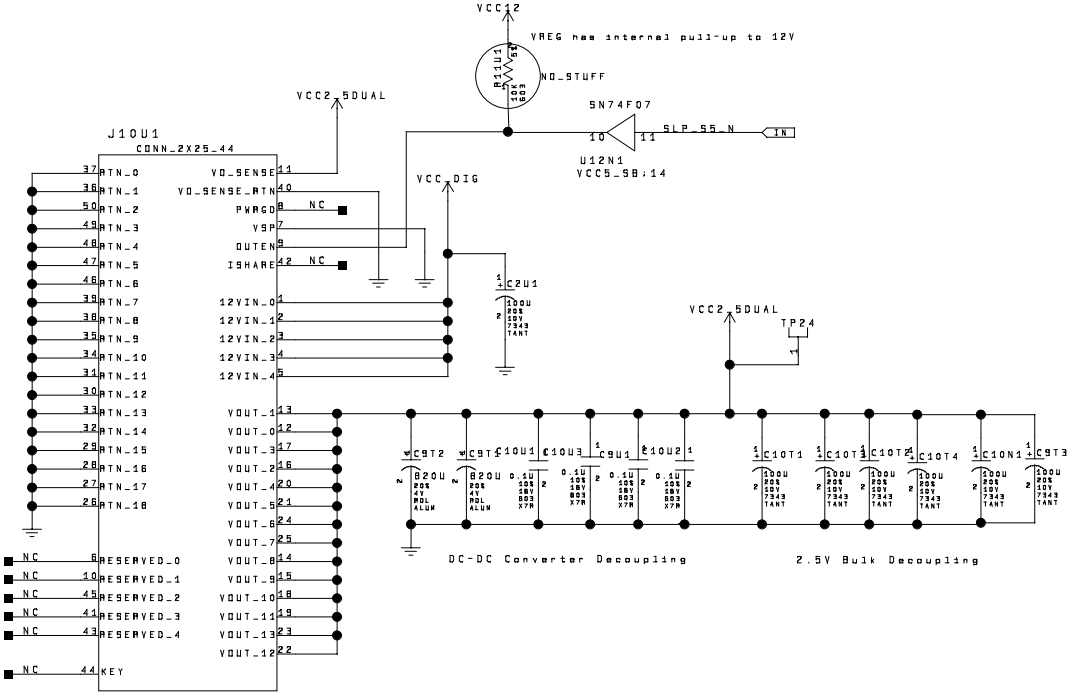
2.5V GENERATION

ROOM=2.5V_GEN



1.8V GENERATION FOR RAMBUS CHB TERM

ROOM=1.8V_GEN

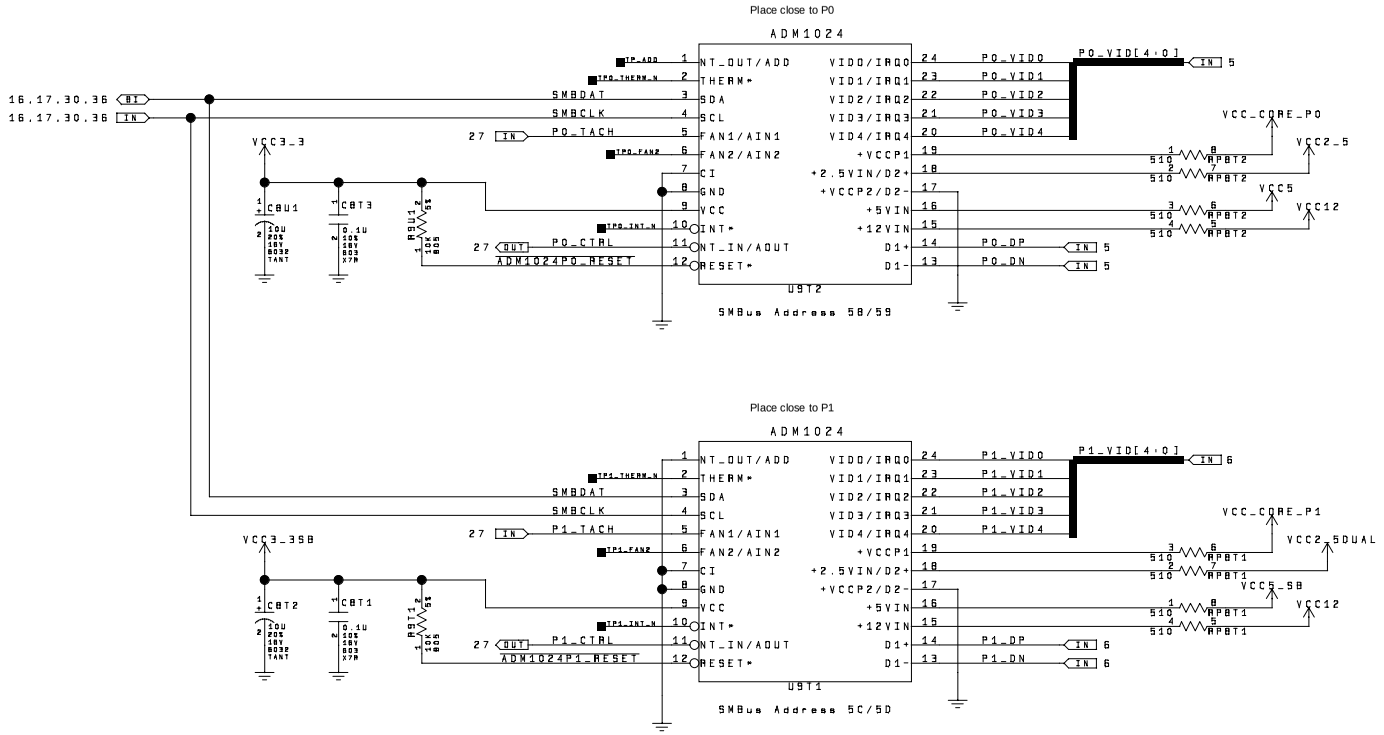


RAMBUS 2.5V DUAL GENERATION

ROOM=RAMBUS_25_GEN

VCC_CMOS / 2.5V / 3.3V REGULATORS

TITLE:		Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 2-4-2000 9:15	OF 53

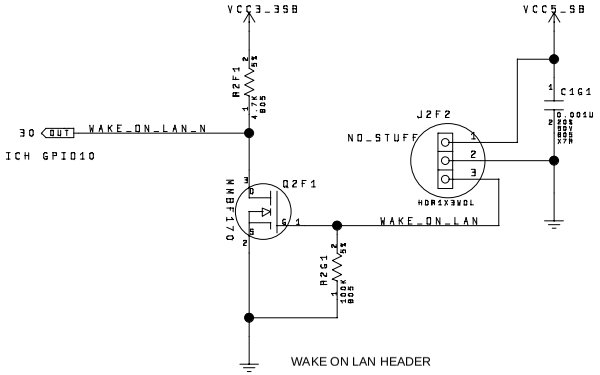


Not Populated

TEMP / VOLTAGE MONITORING

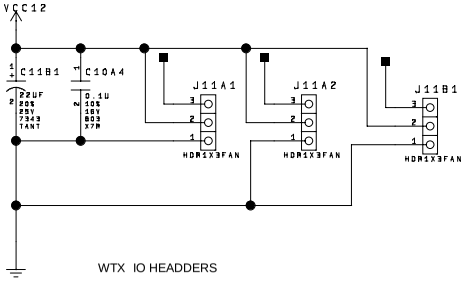
ROOM=PROCESSORS

TITLE:		Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 2-4-2000 9:16	OF 53

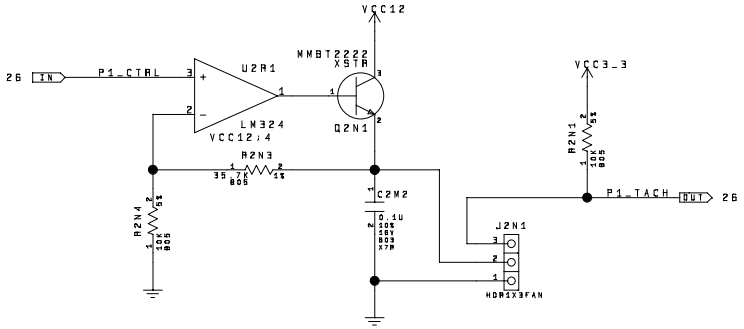


WAKE ON LAN HEADER

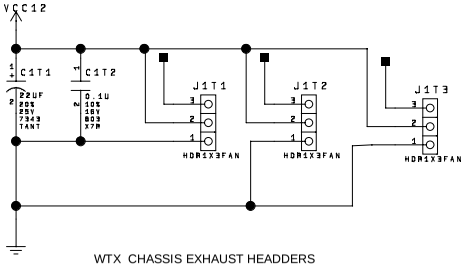
ROOM=82559



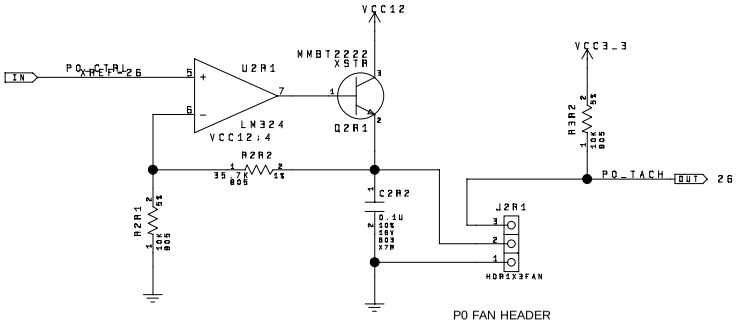
WTX IO HEADDERS



P1 FAN HEADER



WTX CHASSIS EXHAUST HEADDERS

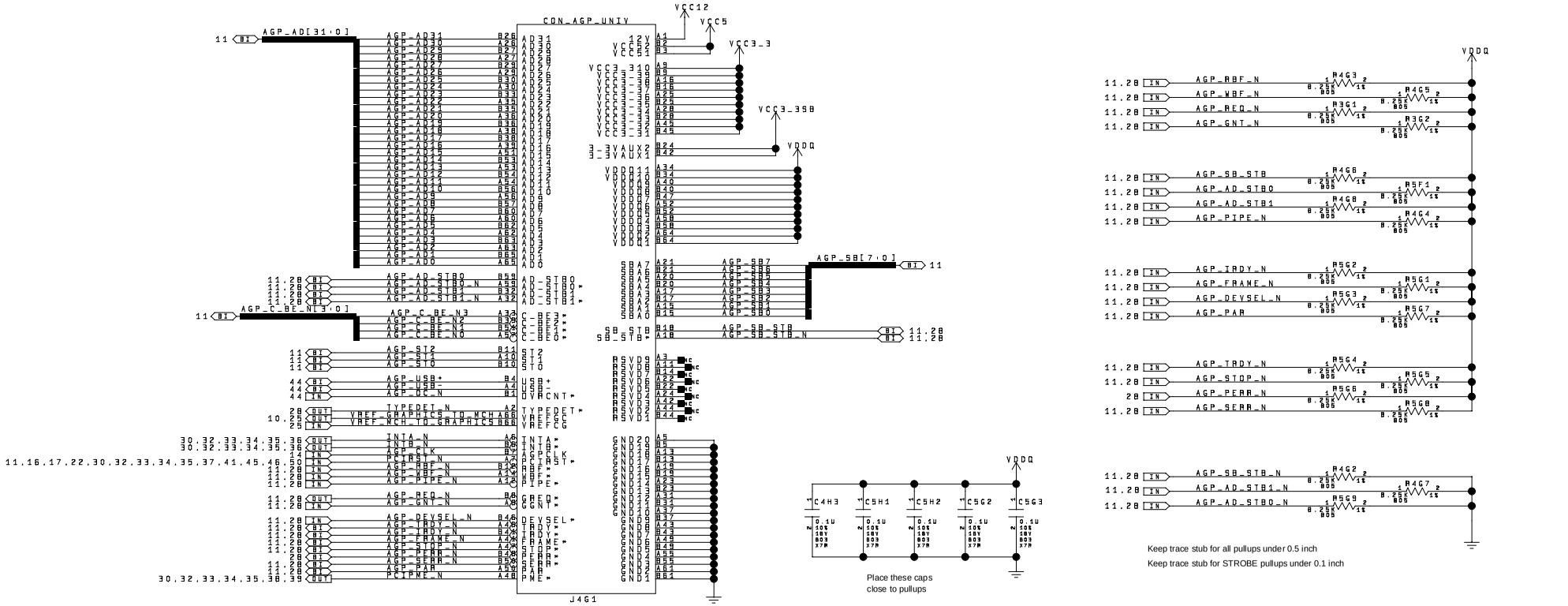


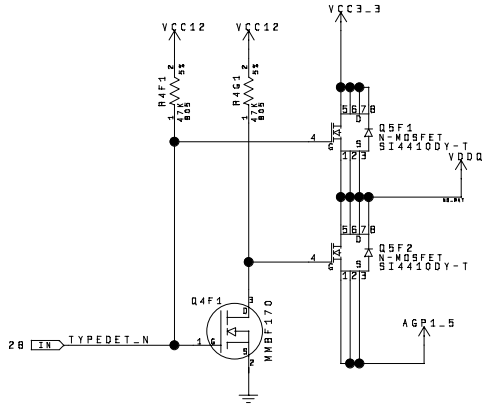
P0 FAN HEADER

ROOM=PROCESSORS

WOL / FAN HEADERS

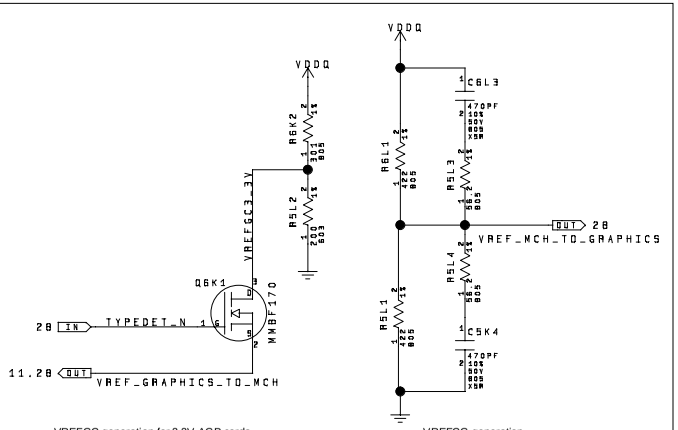
TITLE:		Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 2-4-2000_9:24	OF 53





AGP VDDQ SWITCH

AGP 4X



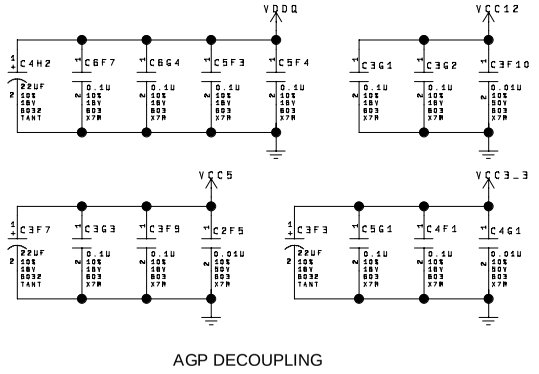
VREFGC generation for 3.3V AGP cards
Place close to MCH

VREFCG generation
Place close to MCH

AGP VREF GENERATION

ROOM=MCH

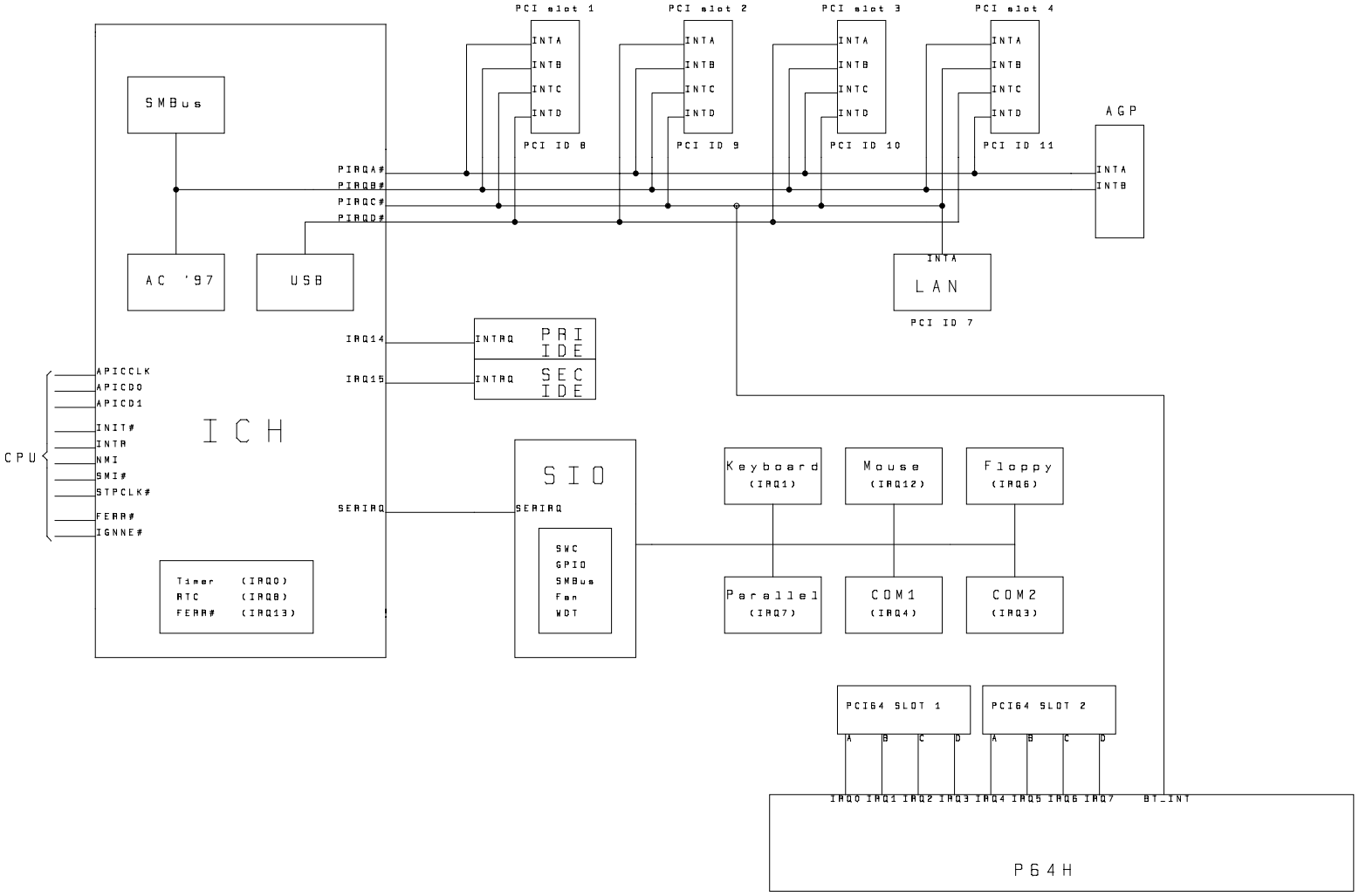
ROOM=AGP4X



AGP DECOUPLING

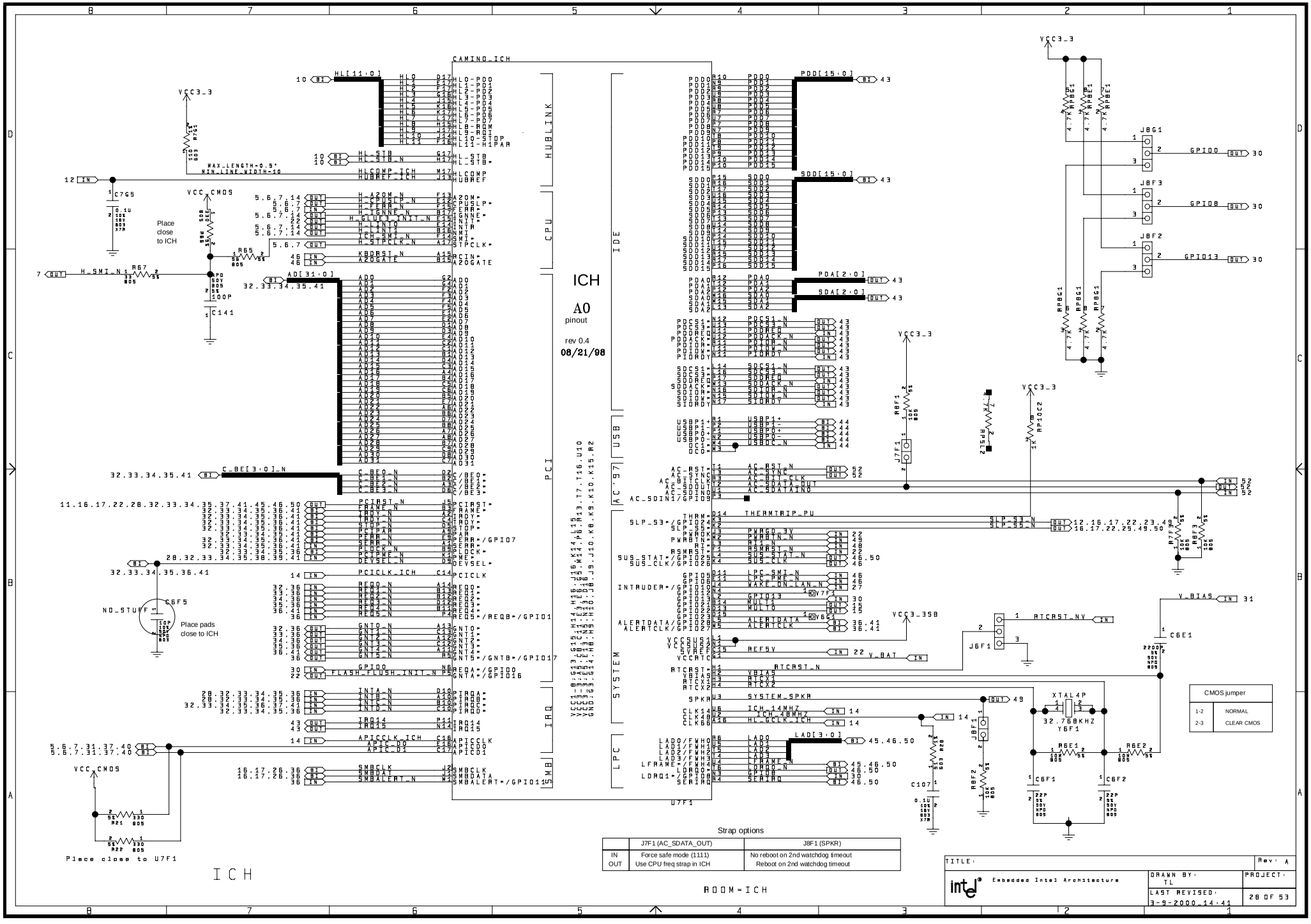
TITLE:	Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
LAST REVISED: 2-4-2000 9:24	26 OF 53

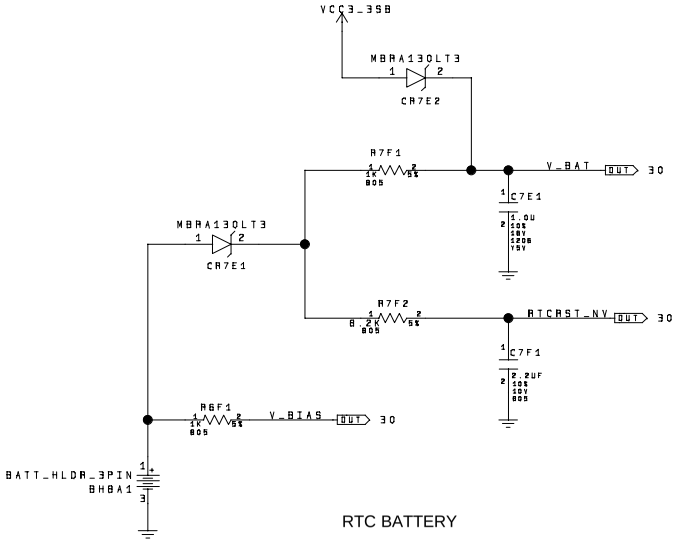
Interrupt Diagram



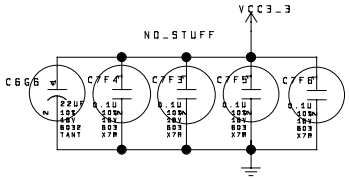
PCI / INTERRUPT DIAGRAM

TITLE:	Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
LAST REVISED: 2-4-2000_9:25	OF 53

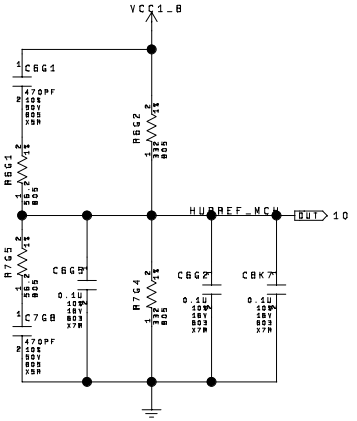

CAMINO_ICH
HUBLINK
CPU
IDE
PCI
USB
AC'97
SYSTEM
IRQ
SMB
LPC
ICH
A0
pinout
rev 0.4
08/21/98
U7F1
Place close to ICH
Place pads close to ICH
NO_STUFF
Place close to U7F1
Strap options
J7F1 (AC_SDATA_OUT)
J8F1 (SPKR)
IN
Force safe mode (1111)
No reboot on 2nd watchdog timeout
OUT
Use CPU freq strap in ICH
Reboot on 2nd watchdog timeout
CMOS jumper
1-2
NORMAL
2-3
CLEAR CMOS
ROOM=ICH
TITLE:
Rev: A
Embedded Intel Architecture
DRAWN BY: TL
PROJECT:
LAST REVISED: 3-9-2000 14:41
28 OF 53



RTC BATTERY

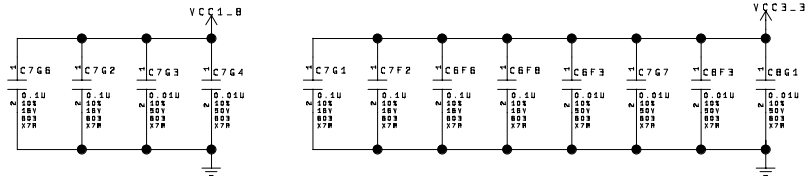


Back No Stuff ICH

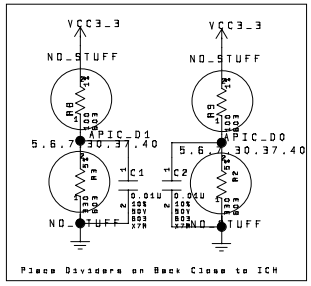


MCH HUBREF GENERATION

Place close to ICH



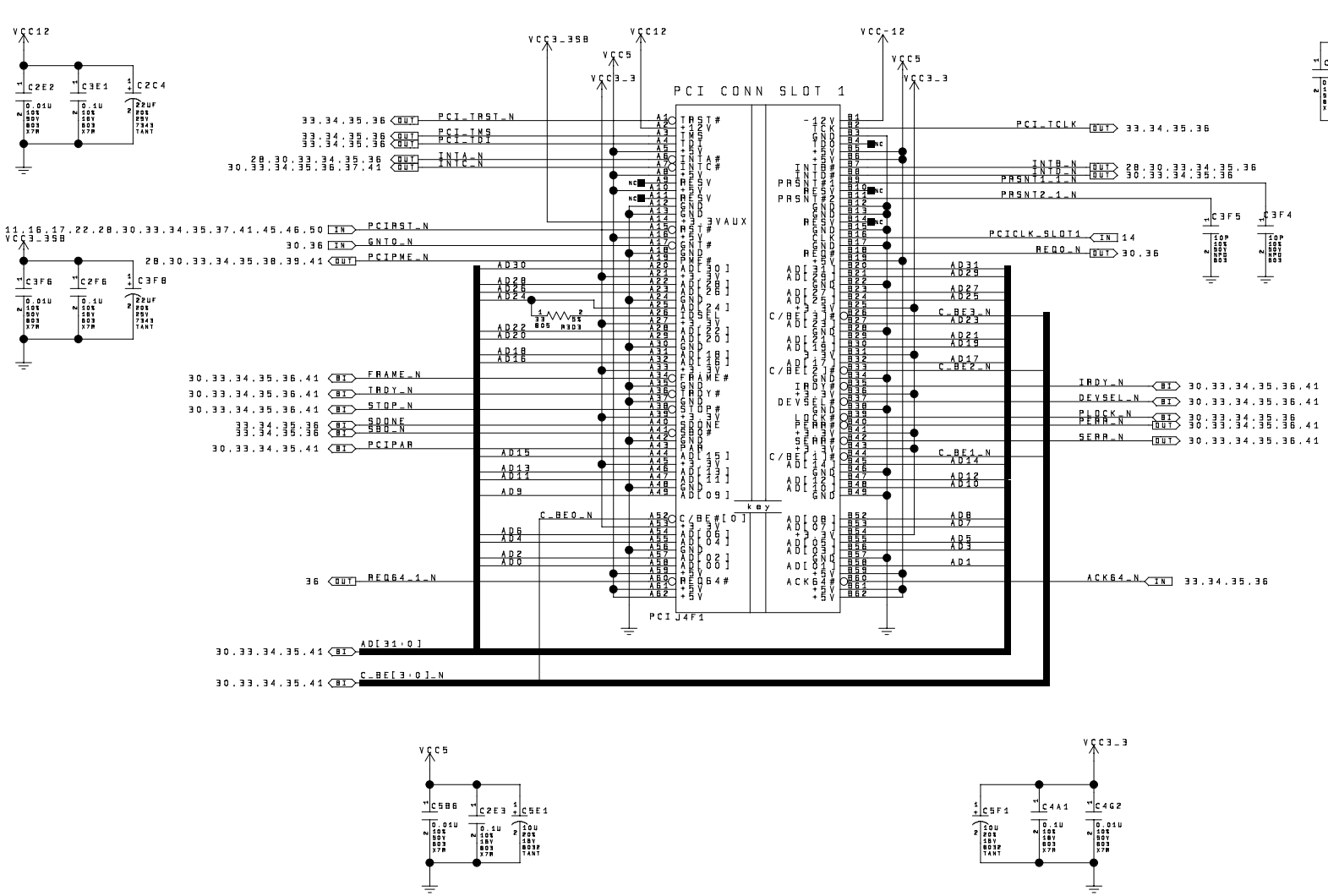
ICH DECOUPLING



ROOM=ICH

ICH DECOUPLING AND SUPPORT CIRCUITRY

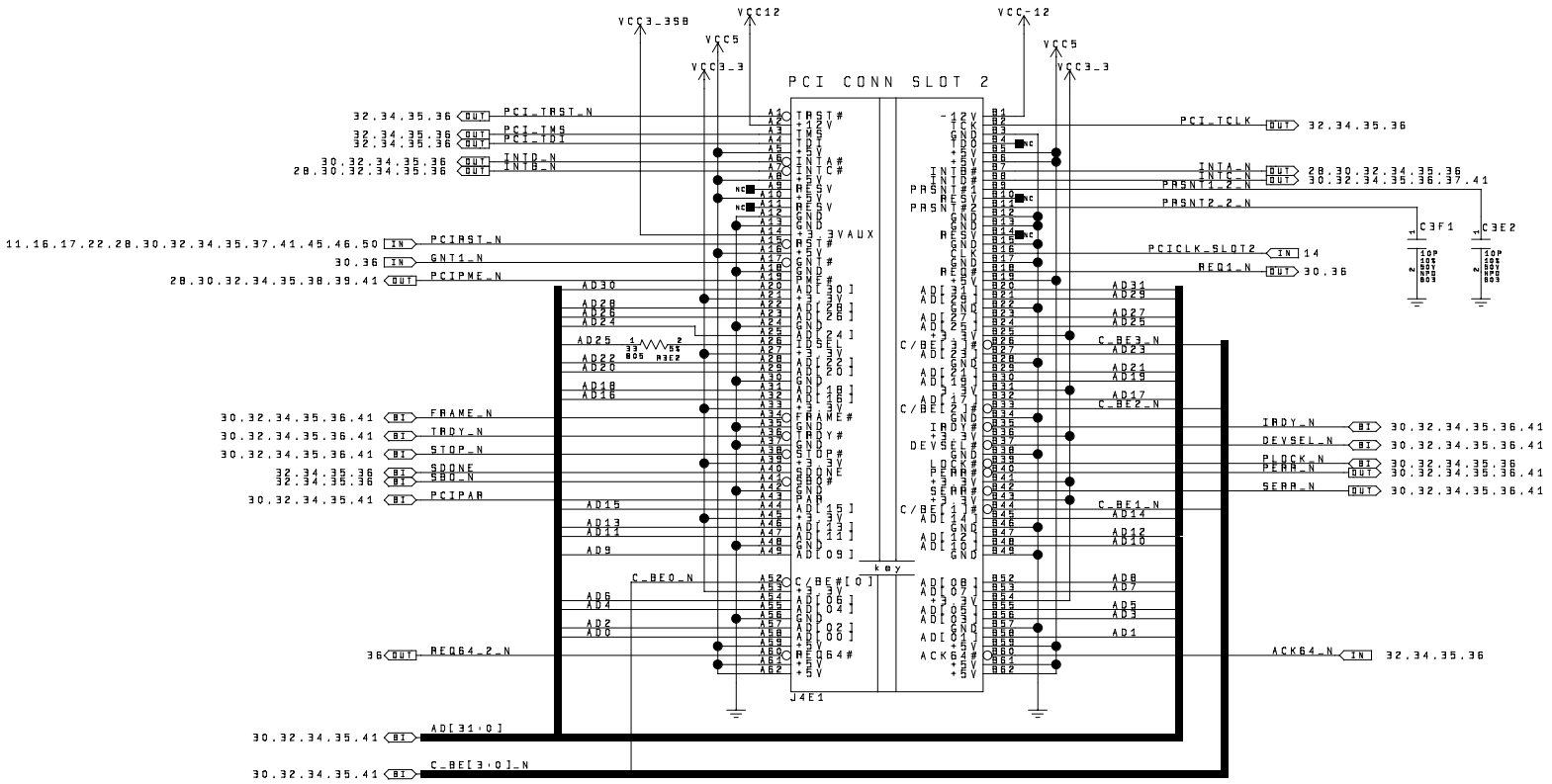
TITLE:	Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
LAST REVISED: 2-4-2000_9:26	29 OF 53



PCI CONN SLOT 1

ROOM=PCI

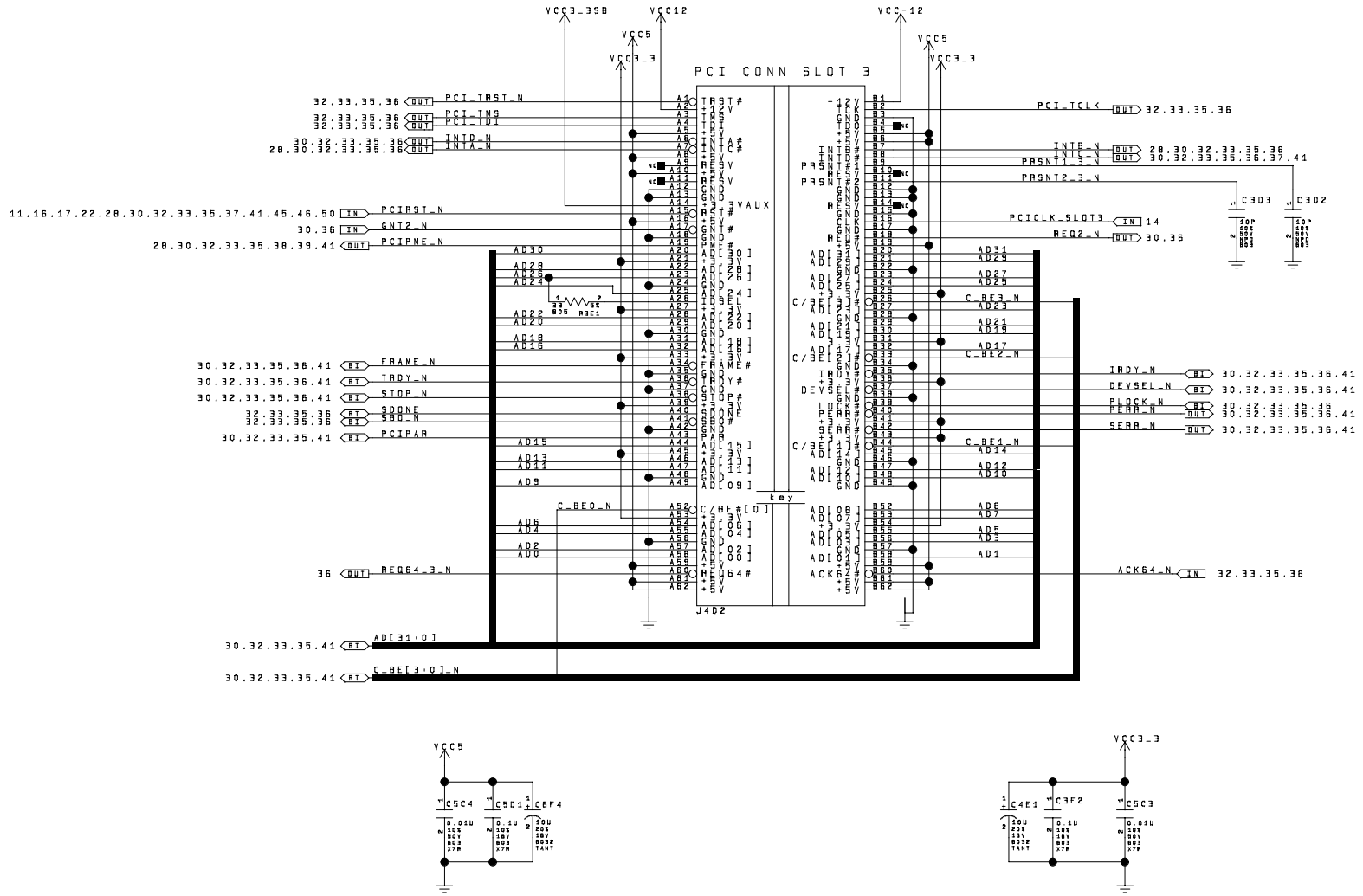
TITLE:	Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
LAST REVISED: 2-4-2000 9:26	30 OF 53



PCI CONN SLOT 2

ROOM=PCI

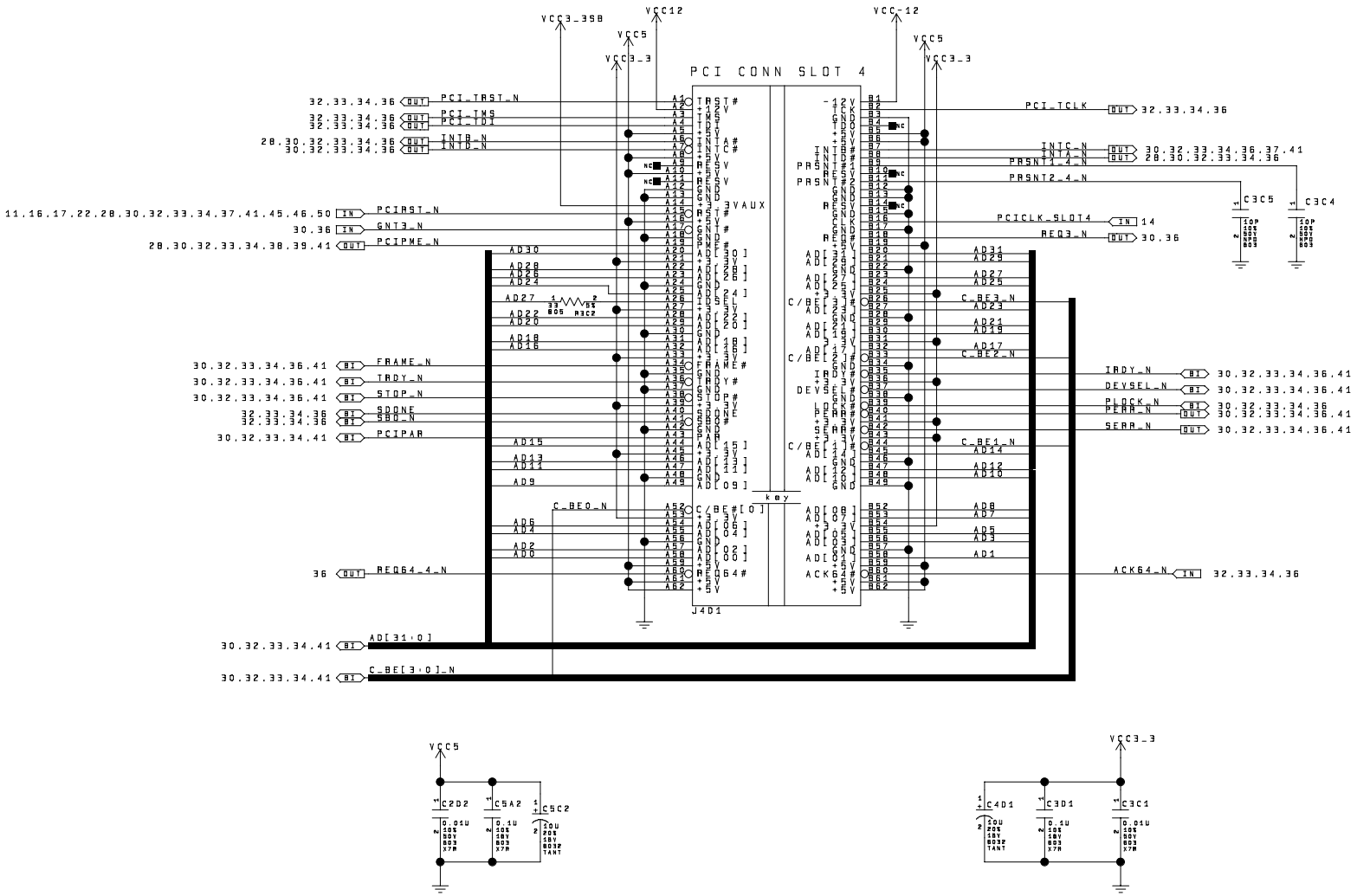
TITLE:	Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
LAST REVISED: 2-4-2000 9:26	31 OF 53



PCI CONN SLOT 3

ROOM=PCI

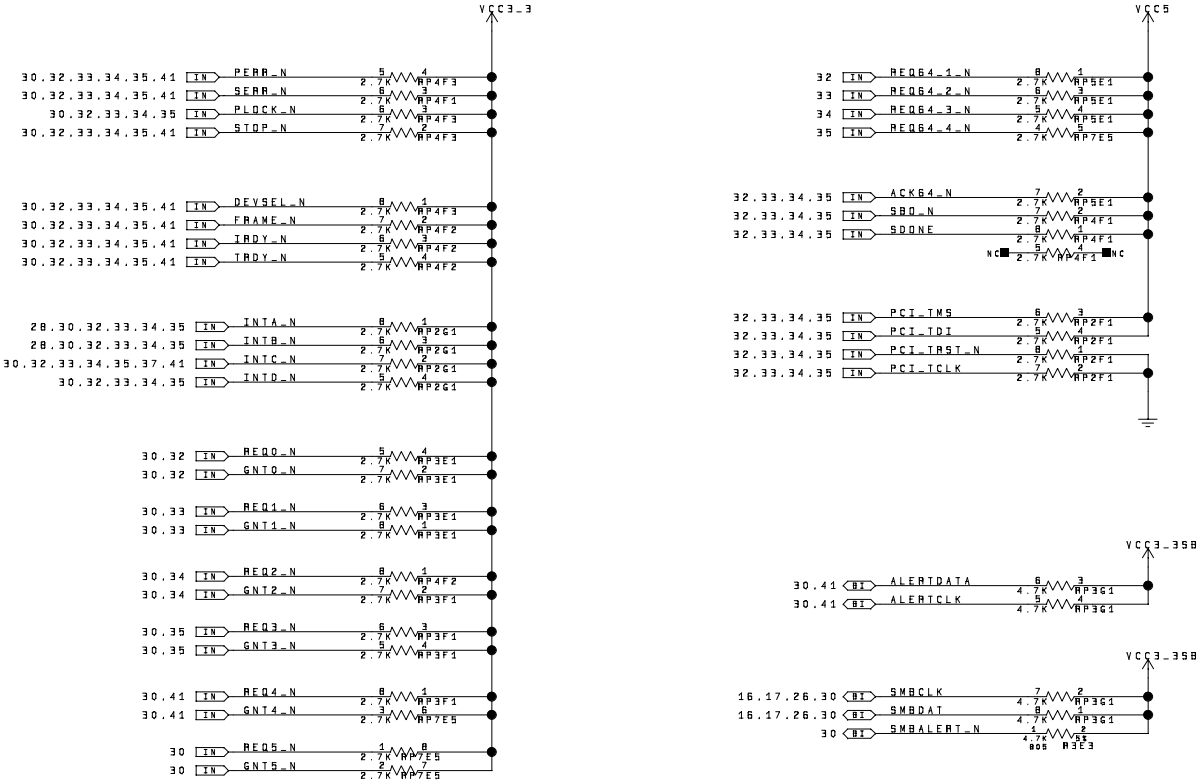
TITLE:	Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
LAST REVISED: 2-4-2000 9:27	32 OF 53



PCI CONN SLOT 4

ROOM=PCI

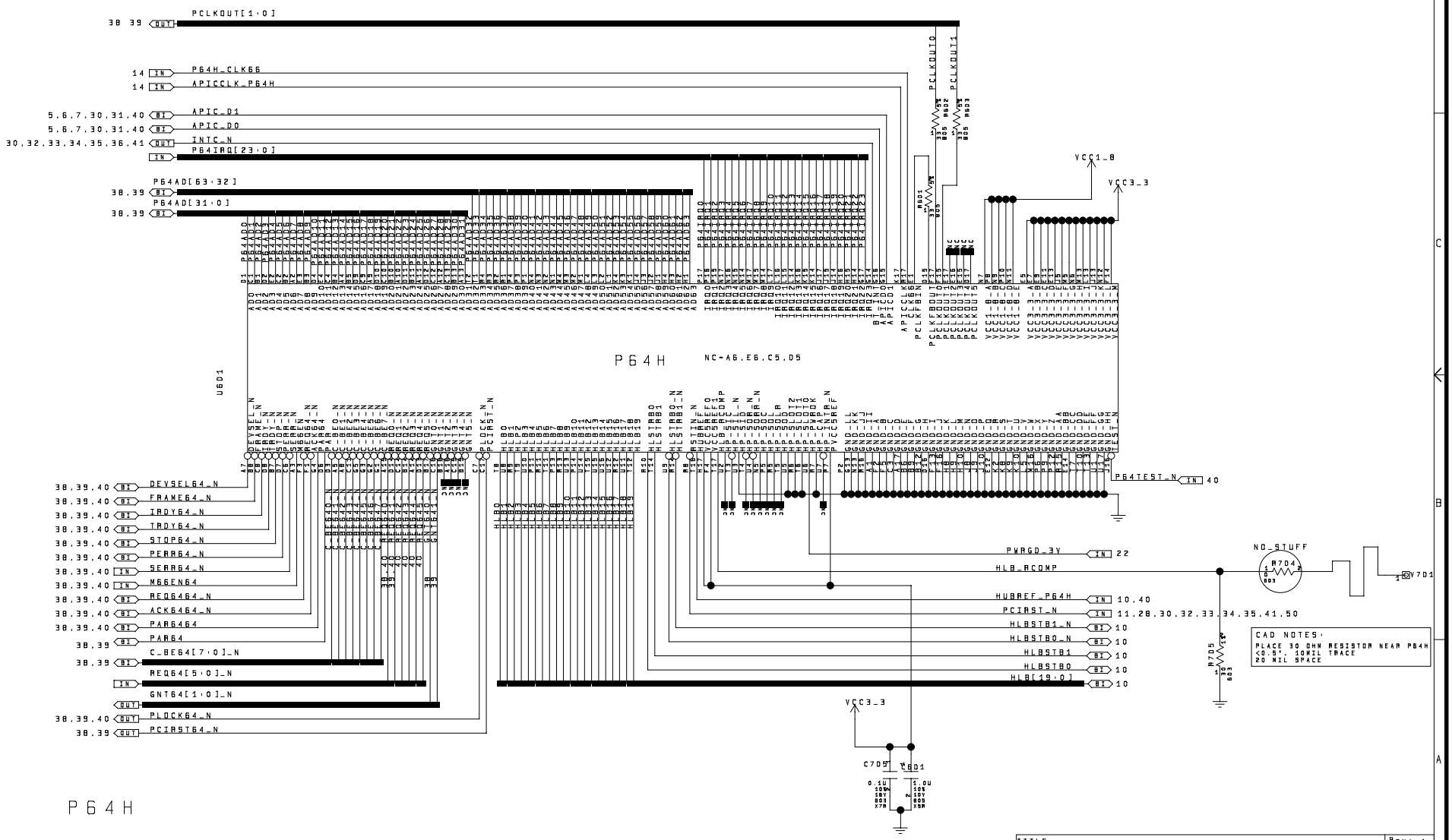
TITLE:	Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
LAST REVISED: 2-4-2000 9:27	33 OF 53



PCI PULLUPS

ROOM=PCI

TITLE:		Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 2-4-2000 9:27	34 OF 53


PCLKOUT[1:0]
38 39 OUT
14 IN P64H_CLK66
14 IN APICCLK_P64H
5,6,7,30,31,40 BI APIC_D1
5,6,7,30,31,40 BI APIC_D0
30,32,33,34,35,36,41 OUT INTC_N
IN P64IRQ[23:0]
P64ADB[63:32]
38,39 BI
P64ADB[31:0]
38,39 BI
U6D1
P64H
NC-A6,E6,C5,D5
VCC1_8
VCC3_3
PCLKOUT0
PCLKOUT1
R601
R602
R603
R604
R605
P64TEST_N IN 40
PWRGD_3V IN 22
HLB_RCOMP
HUBREF_P64H IN 10,40
PCIRST_N IN 11,28,30,32,33,34,35,41,50
HLBSTB1_N BI 10
HLBSTB0_N BI 10
HLBSTB1 BI 10
HLBSTB0 BI 10
HLB[10:0] BI 10
DEVSEL64_N
FRAME64_N
IRDY64_N
TRDY64_N
STOP64_N
PERR64_N
SERR64_N
M66EN64
REQ64A64_N
ACK64A64_N
PAR64A64
PAR64
C_BE64[7:0]_N
REQ64[5:0]_N
GNT64[1:0]_N
PLOCK64_N
PCIRST64_N
NO_STUFF
R704
V701
R705
CAD NOTES:
PLACE 30 OHM RESISTOR NEAR P64H
<0.5", 10MIL TRACE
20 MIL SPACE
C705
C601
0.1U
1.0U
P64H
ROOM=P64H
TITLE:
Rev: A
Embedded Intel Architecture
DRAWN BY: TL
PROJECT:
LAST REVISED: 2-4-2000 9:28
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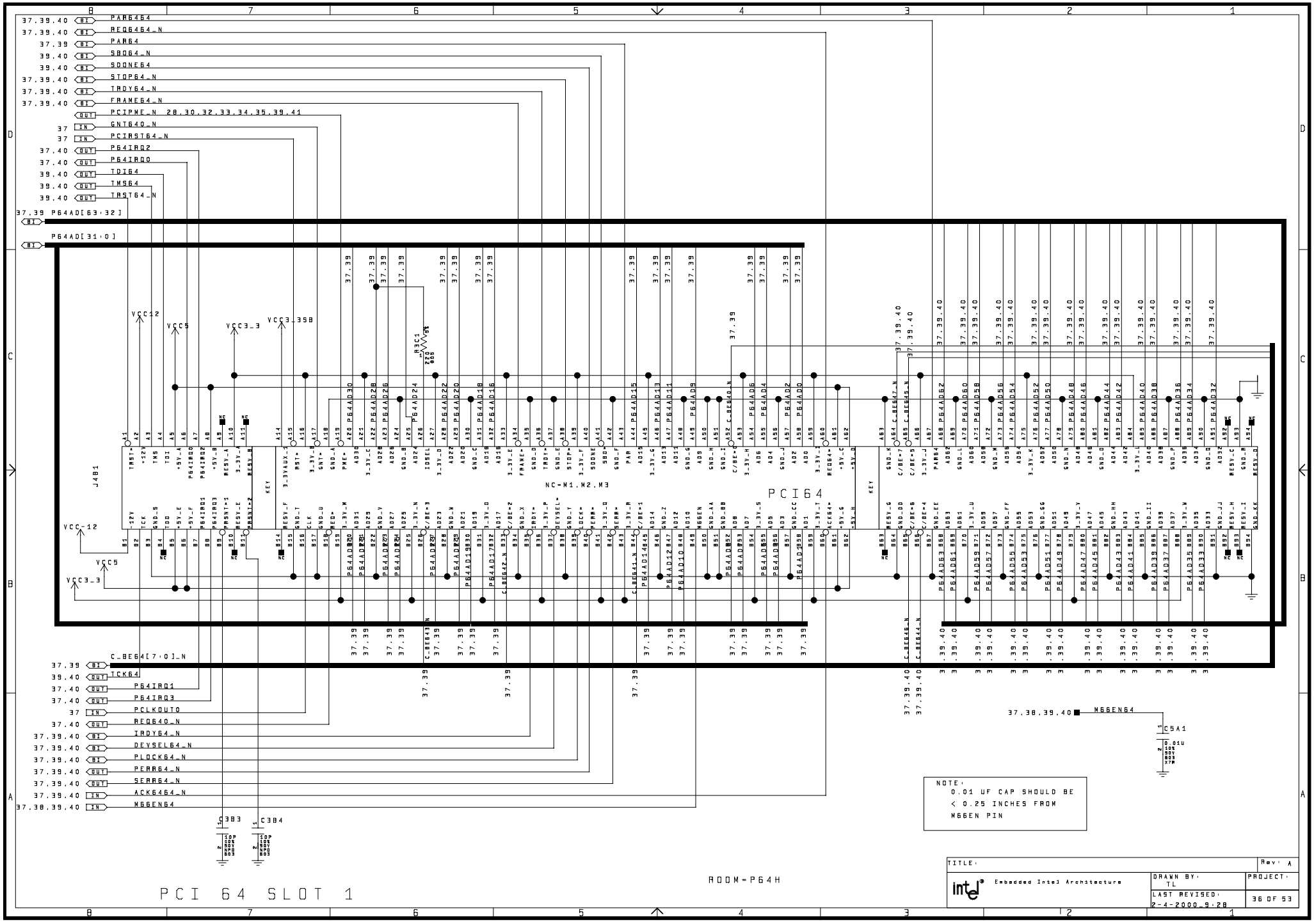
PCI 64 SLOT 1
PCI64
J4B1
NC=M1,M2,M3
KEY
ROOM=P64H
NOTE:
0.01 UF CAP SHOULD BE
< 0.25 INCHES FROM
M66EN PIN
PAR6464
REQ6464_N
PAR64
SBO64_N
SDONE64
STOP64_N
TRDY64_N
FRAME64_N
PCIPME_N 28,30,32,33,34,35,39,41
GNT640_N
PCIRST64_N
P64IRQ2
P64IRQ0
TDI64
TMS64
TRST64_N
P64AD[63:32]
P64AD[31:0]
C_BE64[7:0]_N
TCK64
P64IRQ1
P64IRQ3
PCLKOUT0
REQ640_N
IRDY64_N
DEVSEL64_N
PLOCK64_N
PERR64_N
SERR64_N
ACK6464_N
M66EN64
VCC12
VCC5
VCC3_3
VCC3_3SB
R3C1
220
805
C3B3
C3B4
C5A1
0.01U
10%
50V
X7R
TITLE:
Rev: A
DRAWN BY:
TL
PROJECT:
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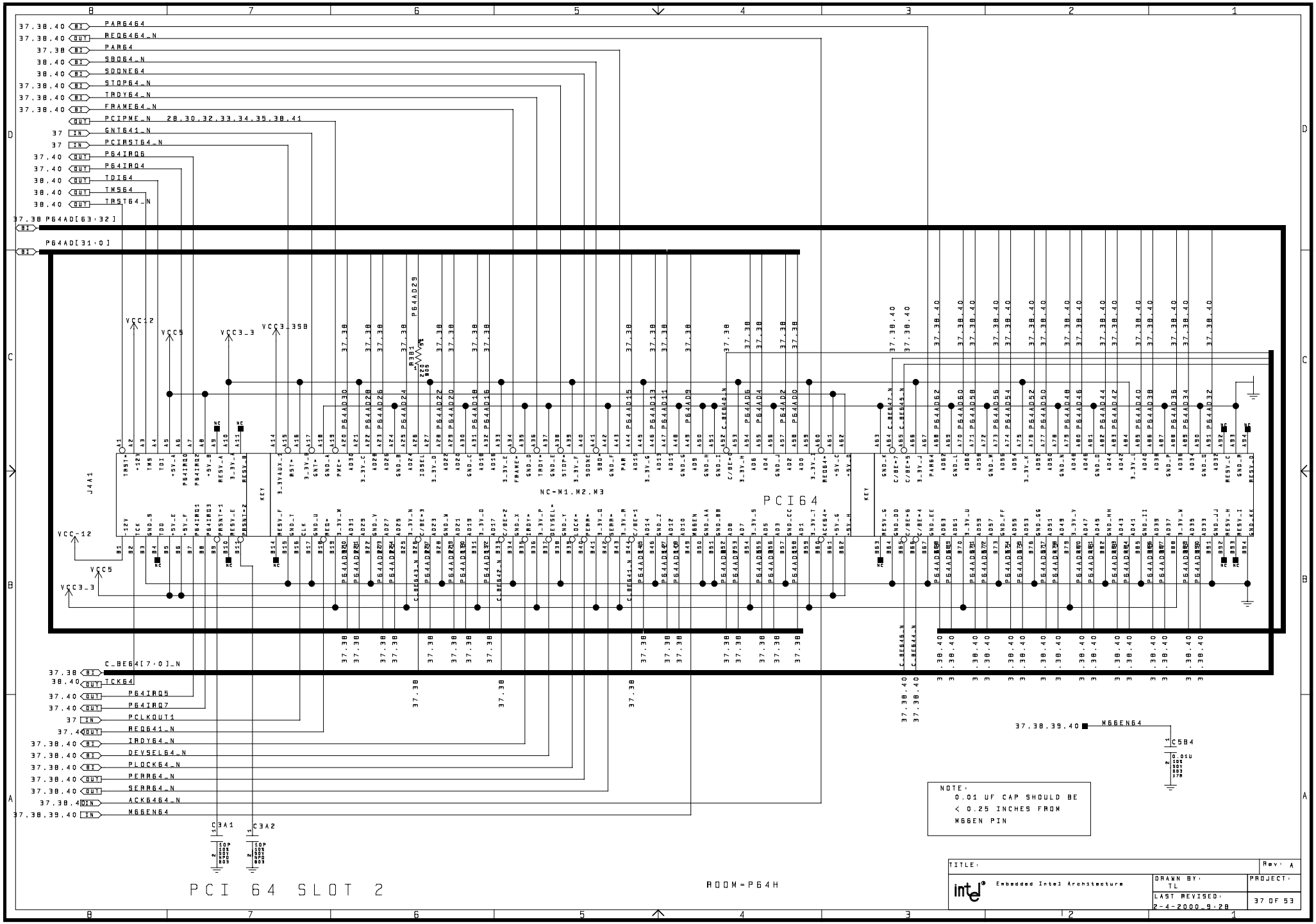
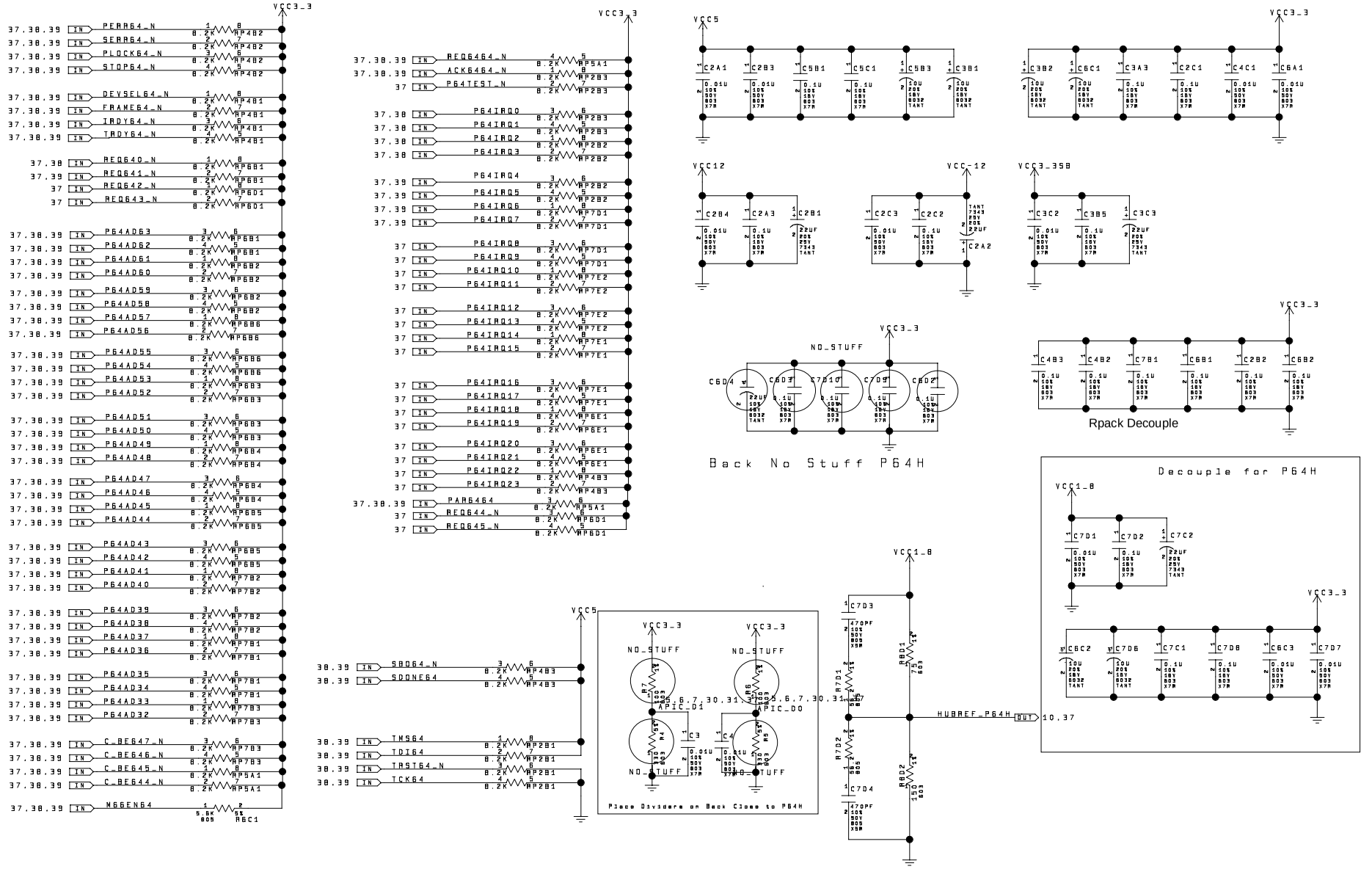
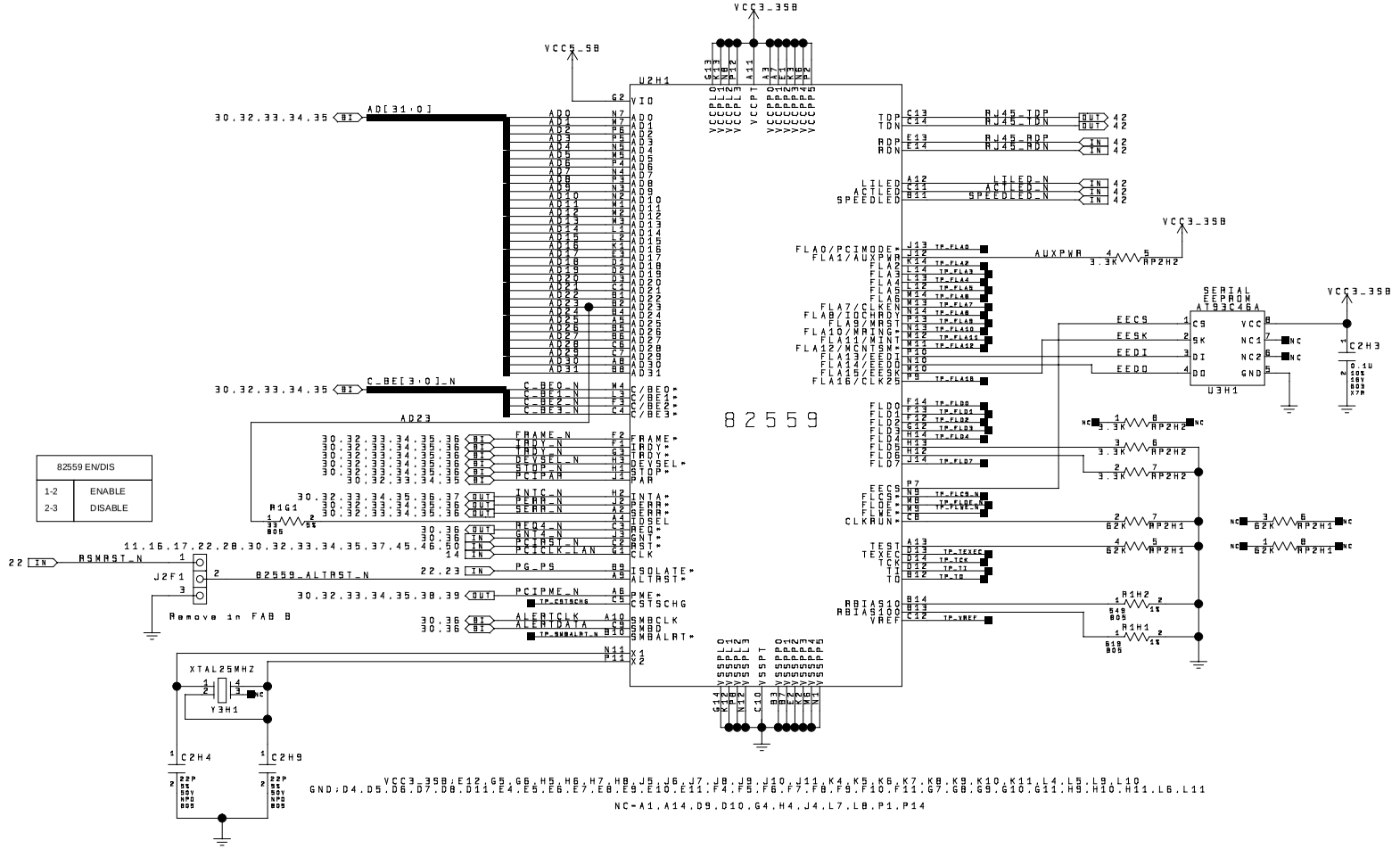
Embedded Intel Architecture


PCI64
PCI 64 SLOT 2
ROOM=P64H
NC-M1.M2.M3
KEY
J4A1
P64AD[63:32]
P64AD[31:0]
C_BE64[7:0]_N
PAR6464
REQ6464_N
PAR64
SBO64_N
SDONE64
STOP64_N
TRDY64_N
FRAME64_N
PCIPME_N 28,30,32,33,34,35,38,41
GNT641_N
PCIRST64_N
P64IRQ6
P64IRQ4
TDI64
TMS64
TRST64_N
TCK64
P64IRQ5
P64IRQ7
PCLKOUT1
REQ641_N
IRDY64_N
DEVSEL64_N
PLOCK64_N
PERR64_N
SERR64_N
ACK6464_N
M66EN64
C3A1
C3A2
C584
0.01U
NOTE:
0.01 UF CAP SHOULD BE
< 0.25 INCHES FROM
M66EN PIN
TITLE:
Rev: A
Embedded Intel Architecture
DRAWN BY:
TL
PROJECT:
LAST REVISED:
2-4-2000 9:28
37 OF 53



PCI 64/66 PULLUPS AND DECOUPLING

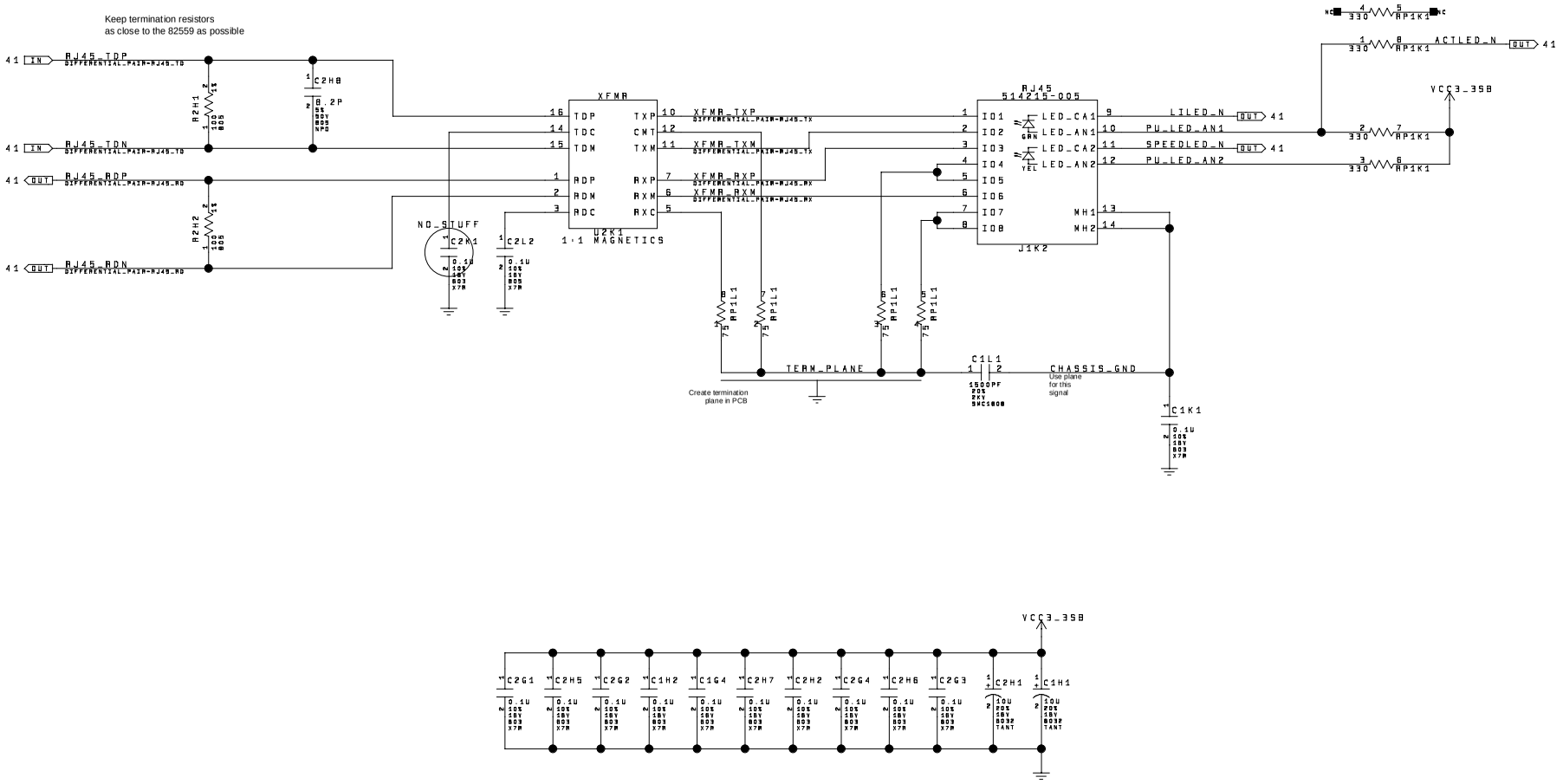
TITLE:	Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
	LAST REVISED: 2-4-2000 9:29
	38 OF 53



ETHERNET 82559ER

ROOM=82559

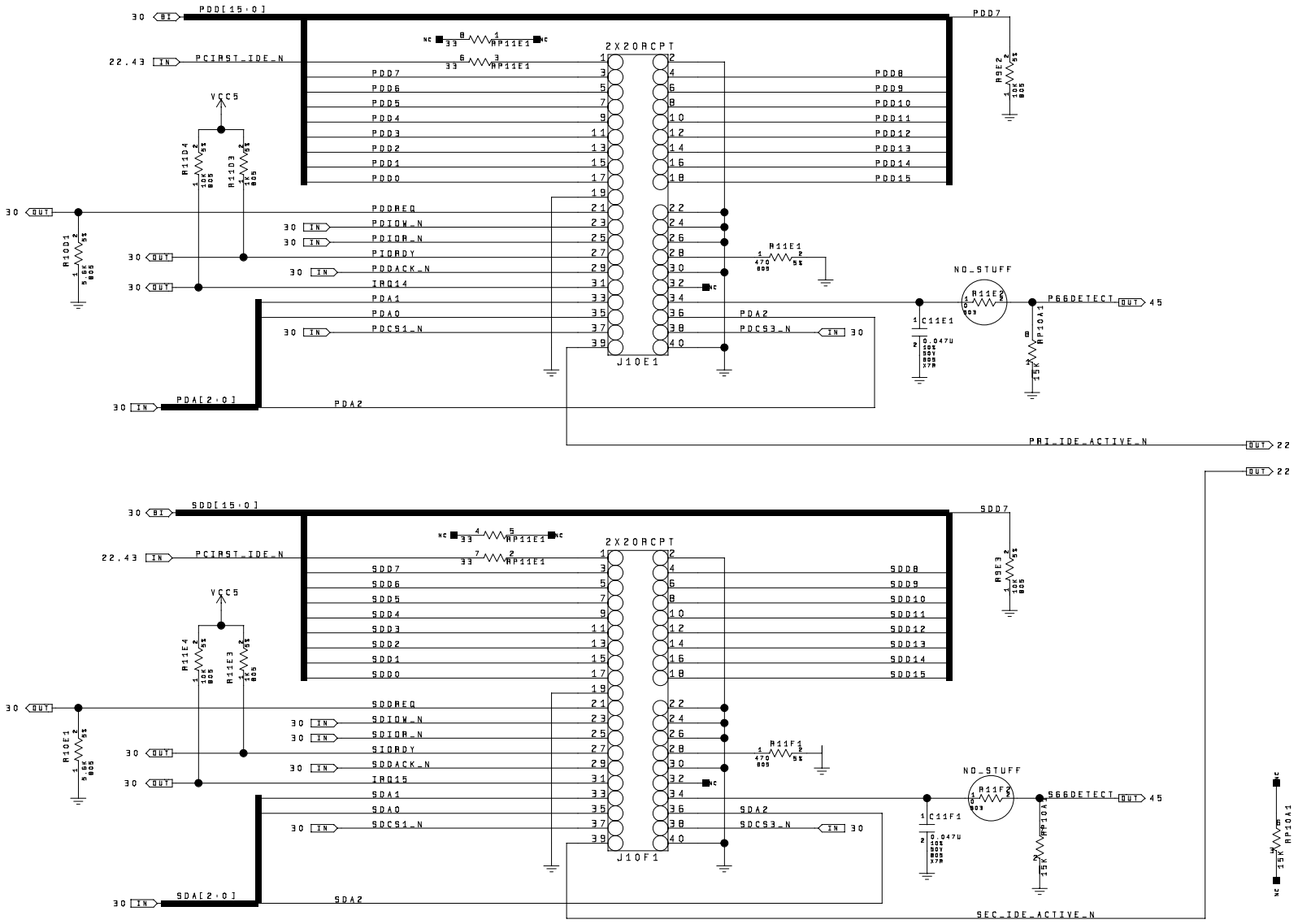
TITLE:	Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
	LAST REVISED: 2-4-2000,9:29
	39 OF 53



ETHERNET CONNECTOR / DECOUPLING

ROOM=82559

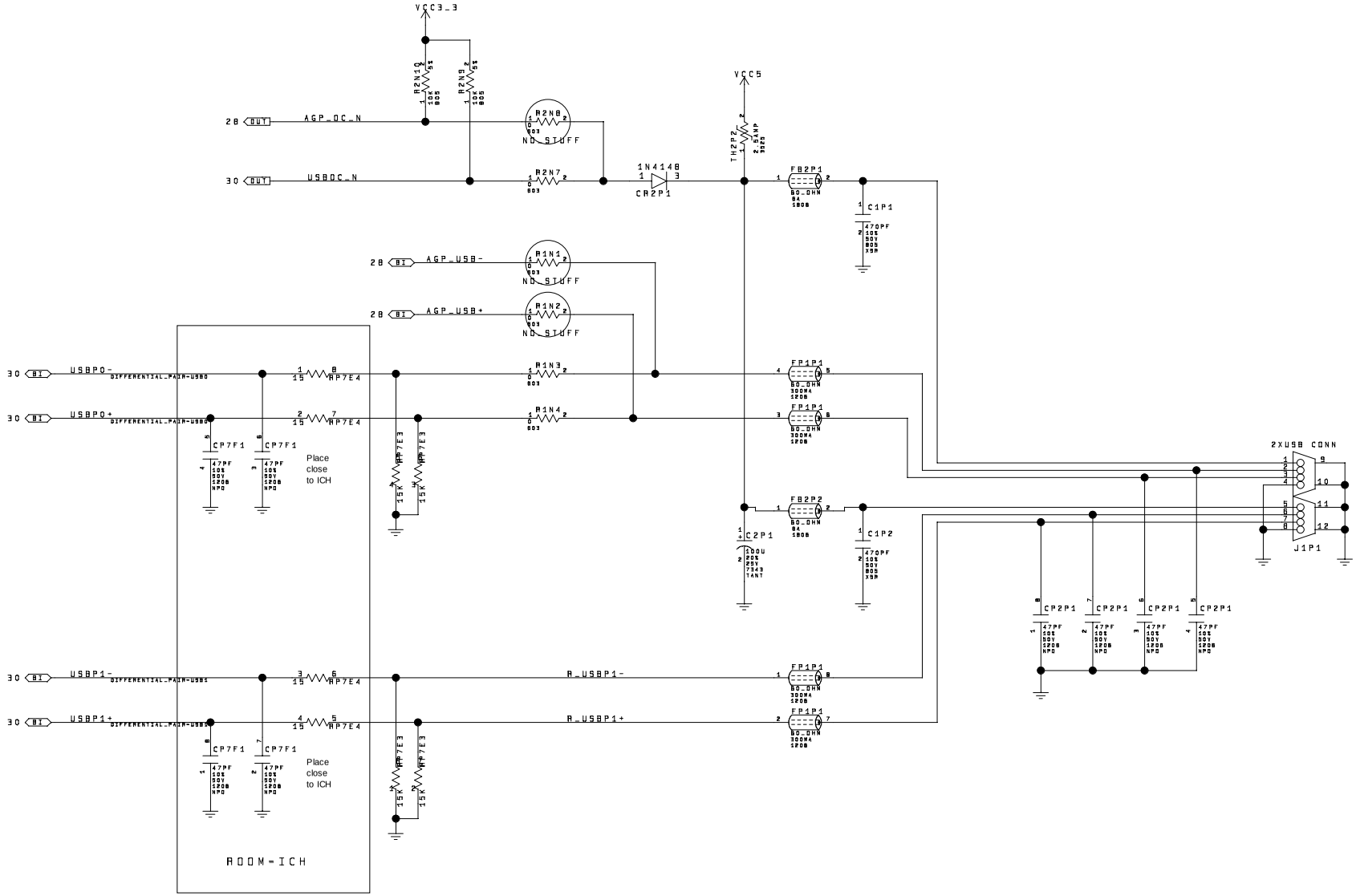
TITLE:		Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 2-4-2000 9:29	40 OF 53



IDE CONNECTORS

ROOM=IDE_CONN

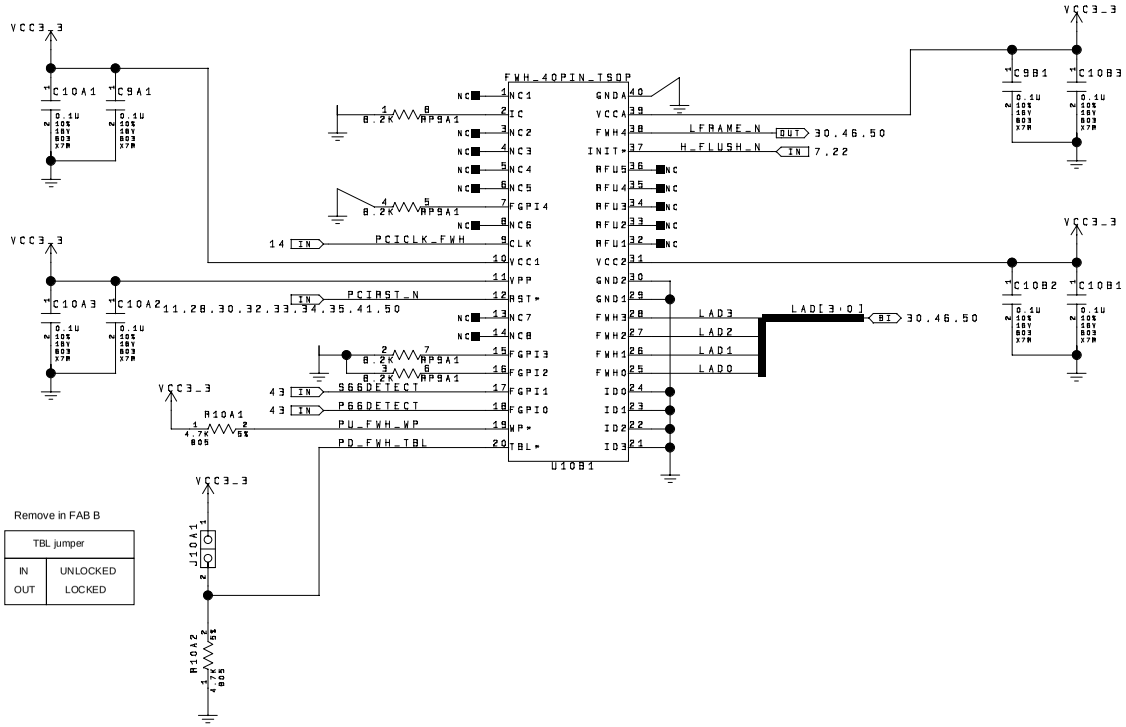
TITLE:		Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 2-4-2000 9:30	41 OF 53



USB CONNECTORS

ROOM=USB_CONN

TITLE:	Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
LAST REVISED: 2-4-2000 9:30	42 OF 53



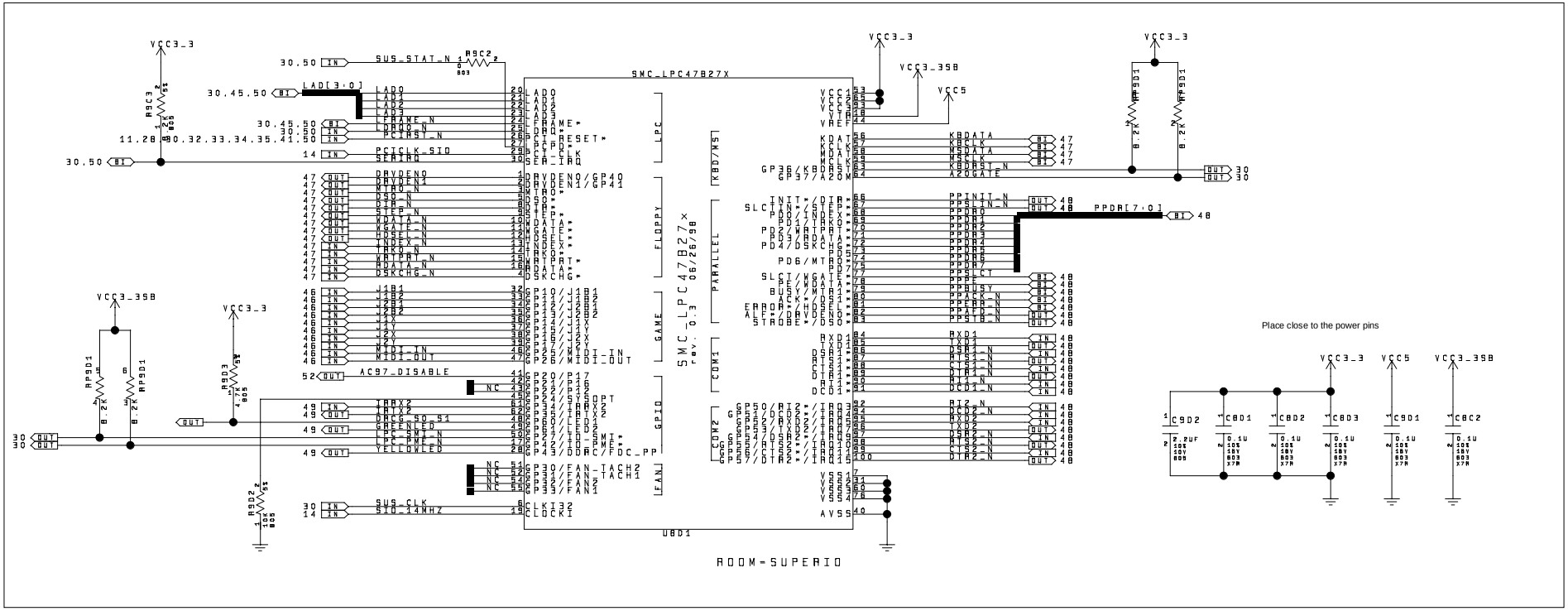
Remove in FAB B

TBL jumper	
IN	UNLOCKED
OUT	LOCKED

F W H

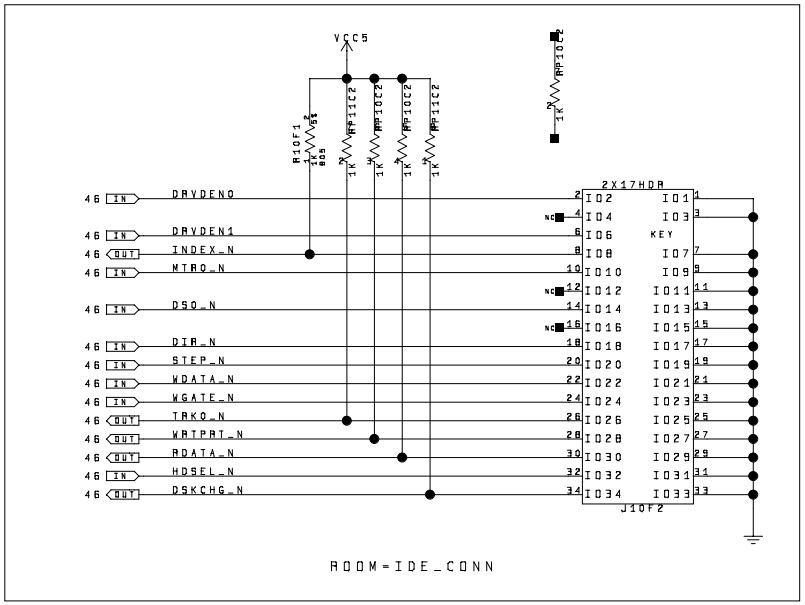
ROOM=FWH

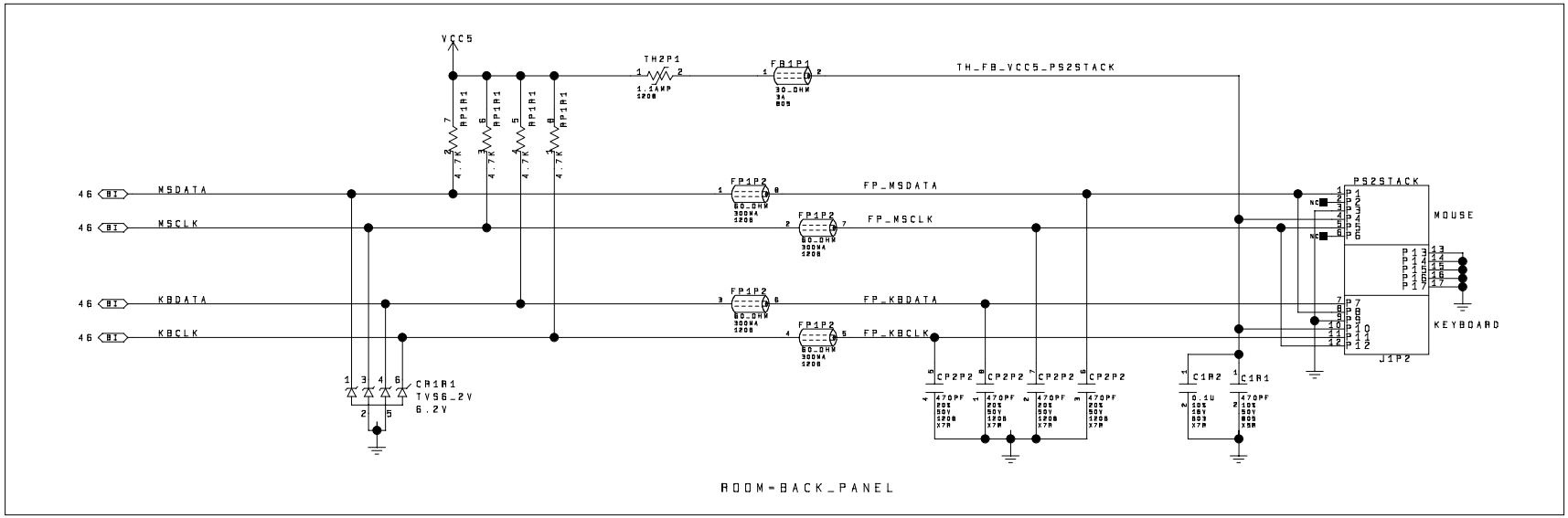
TITLE:		Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 2-4-2000_9:30	43 OF 53



LPC SIO / GAMEPORT HEADER

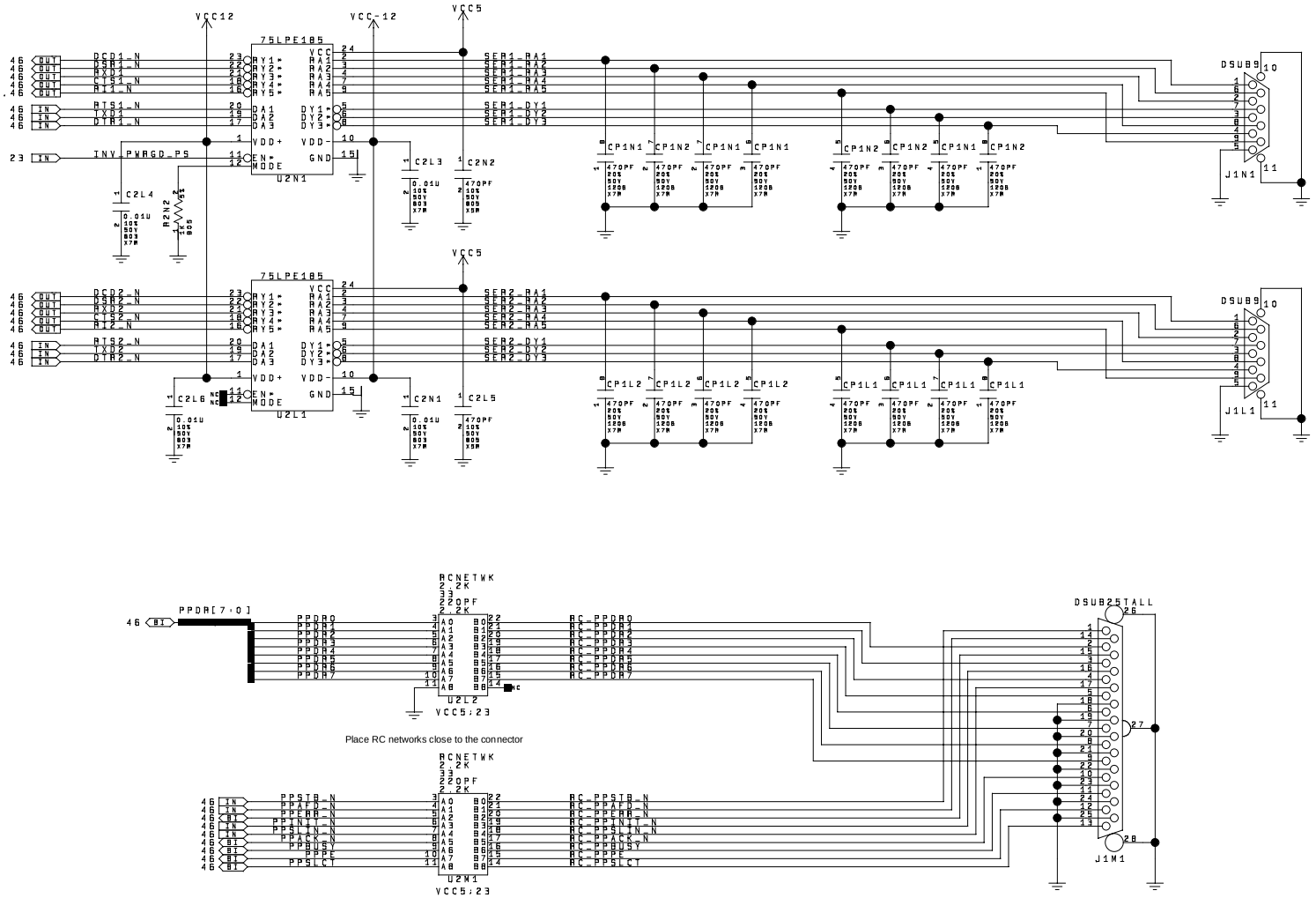
TITLE:	Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
LAST REVISED: 2-4-2000 9:31	44 OF 53





FLOPPY / KBD / MOUSE CONN

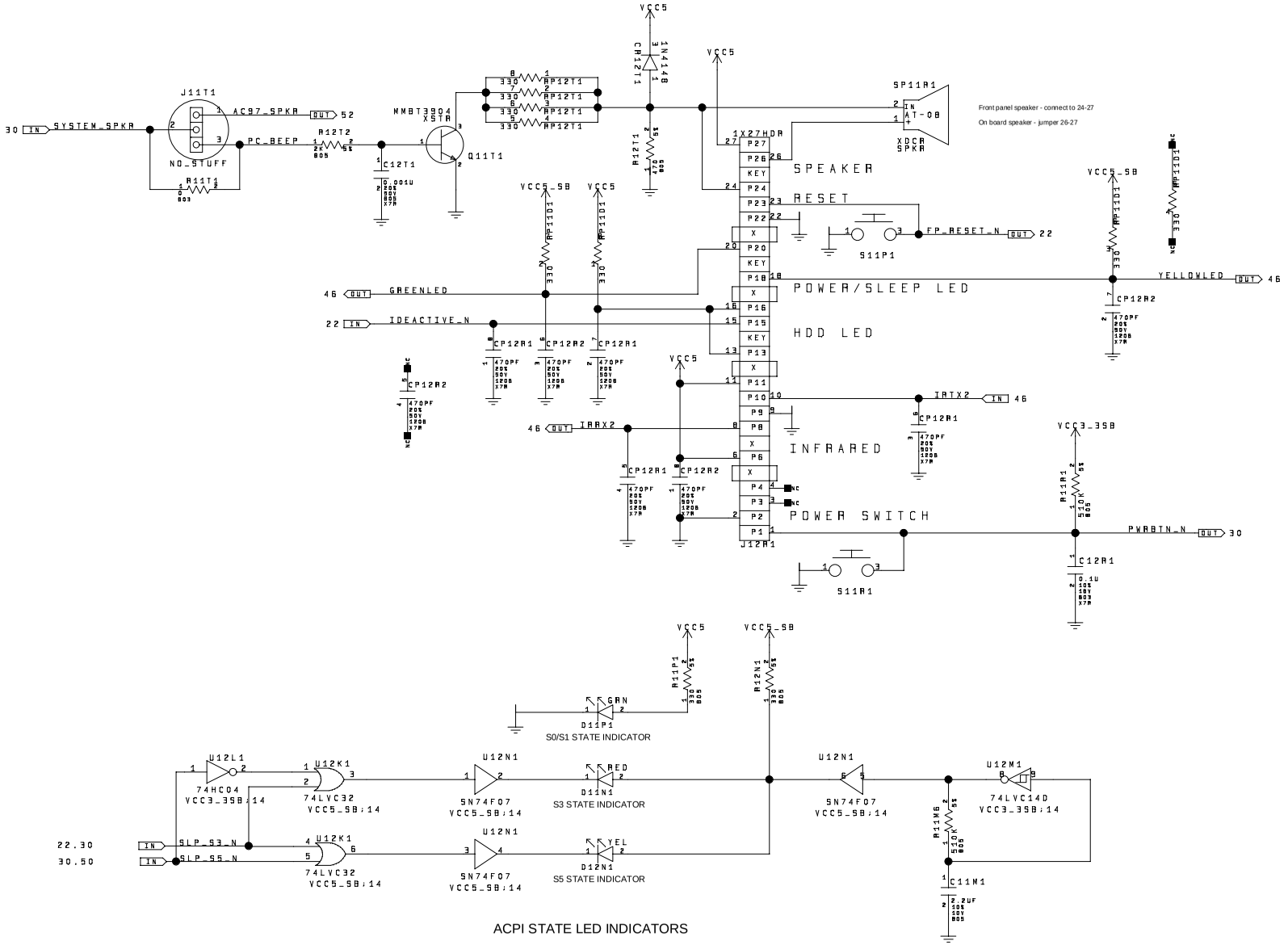
TITLE:		Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 2-4-2000_9:31	45 OF 53



SERIAL / PARALLEL CONN

ROOM=BACK_PANEL

TITLE:	Rev: A
Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
LAST REVISED: 2-4-2000 9:31	46 OF 53

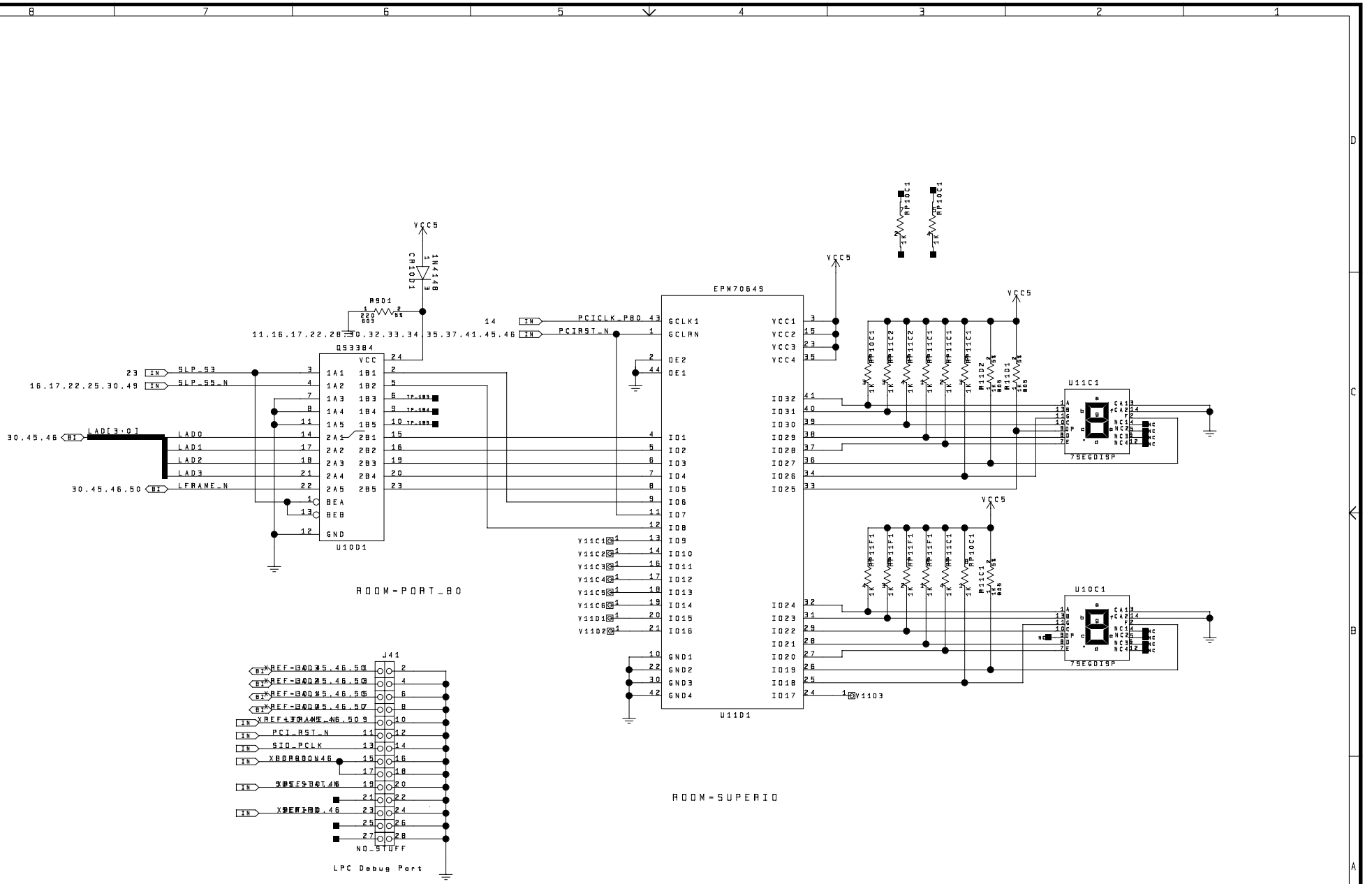


ACPI STATE LED INDICATORS

ROOM=FRONT_PANEL

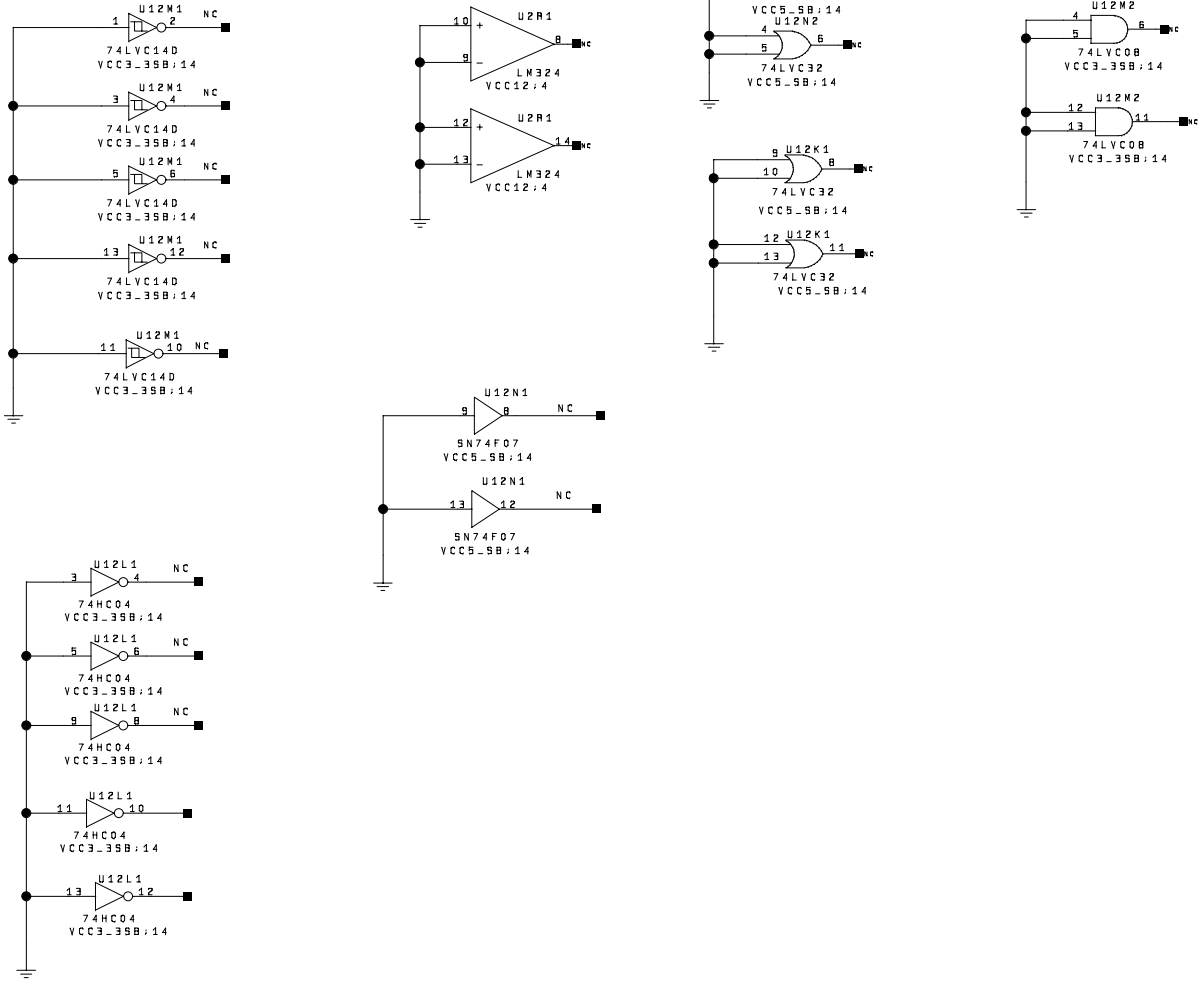
FRONT PANEL CONNECTOR / SPEAKER / ACPI LEDS

TITLE:	Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
LAST REVISED: 2-4-2000 9:32	47 OF 53



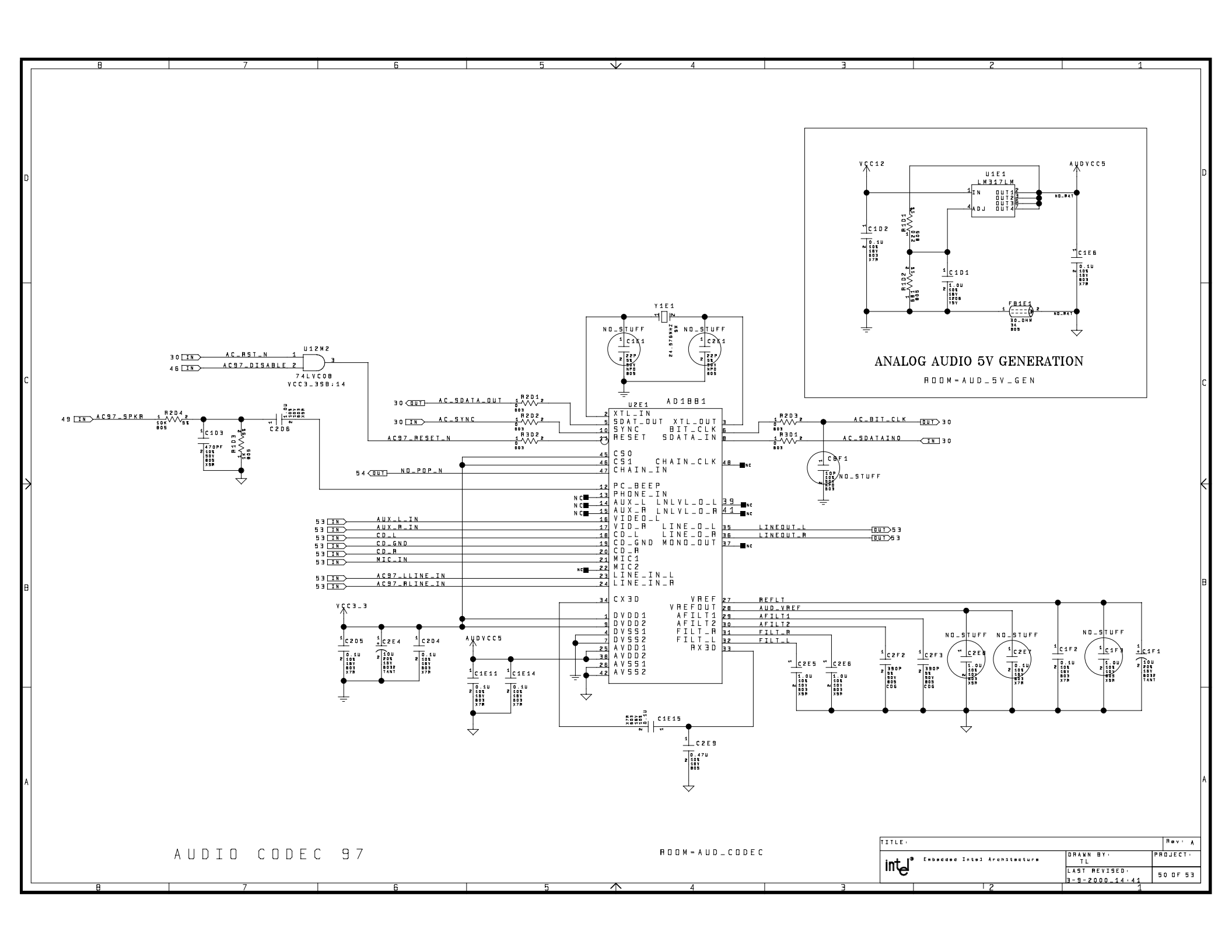
LPC / PORT 80 DISPLAY

TITLE:		Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 2-4-2000 9:32	48 OF 53



SPARE LOGIC

TITLE:		Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 2-4-2000 9:33	49 OF 53


ANALOG AUDIO 5V GENERATION
ROOM=AUD_5V_GEN
U1E1
LM317LM
VCC12
AUDVCC5
ADJ
C1D2
0.1U
R1D1
220
R1D2
680
C1D1
1.0U
C1E6
0.1U
FB1E1
30_OHM
NO_STUFF
AUDIO CODEC 97
ROOM=AUD_CODEC
AD1881
U2E1
Y1E1
24.576MHZ
C1E1
C2E1
22P
AC_RST_N
AC97_DISABLE
74LVC08
VCC3_3SB;14
AC_SDATA_OUT
AC_SYNC
AC97_RESET_N
AC97_SPKR
C1D3
470PF
R1D3
C2D6
NO_POP_N
AC_BIT_CLK
AC_SDATAIN0
C2F1
10P
AUX_L_IN
AUX_R_IN
CD_L
CD_GND
CD_R
MIC_IN
AC97_LLINE_IN
AC97_RLINE_IN
LINEOUT_L
LINEOUT_R
VCC3_3
AUDVCC5
C2D5
C2E4
C2D4
C1E11
C1E14
C1E15
C2E9
0.47U
C2E5
C2E6
C2F2
C2F3
C2E8
C2E7
C1F2
C1F3
C1F1
REFLT
AUD_VREF
AFILT1
AFILT2
FILT_R
FILT_L
TITLE:
Rev: A
Embedded Intel Architecture
DRAWN BY: TL
PROJECT:
LAST REVISED: 3-9-2000 14:41
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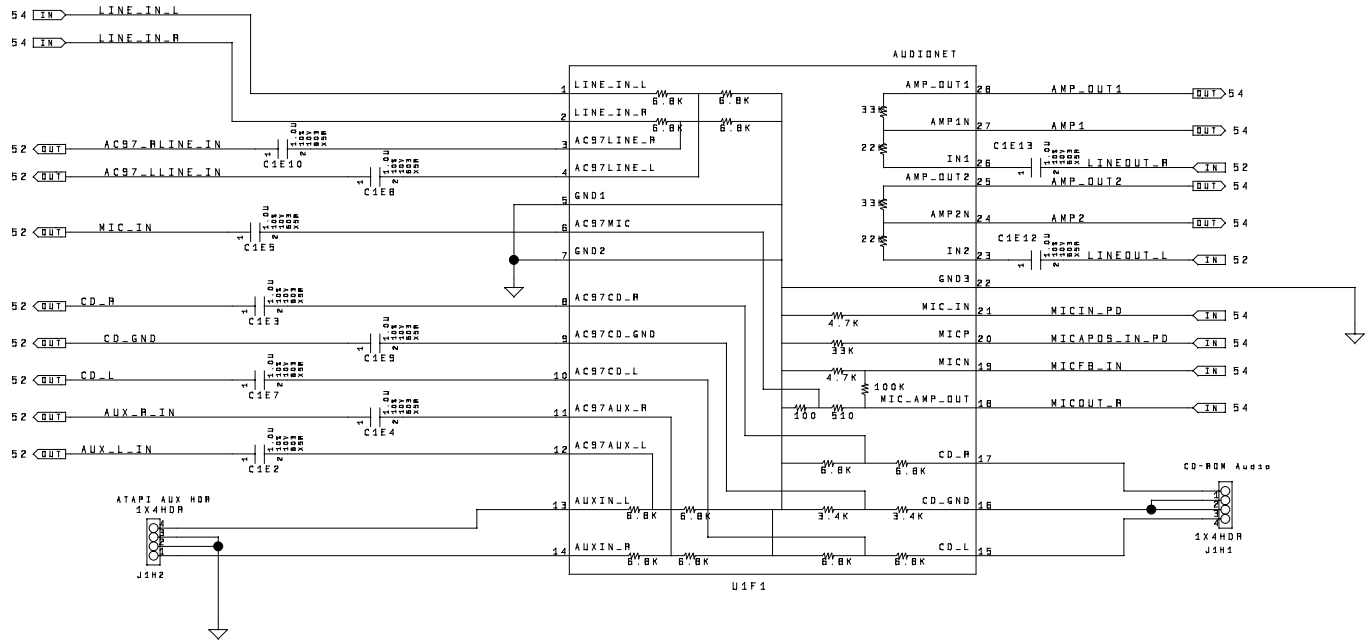
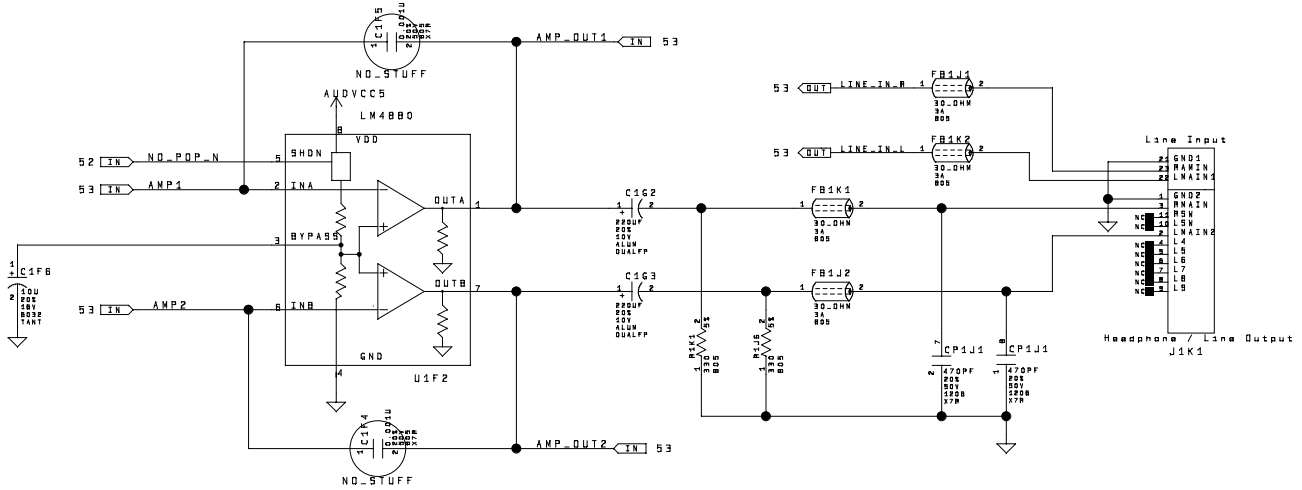
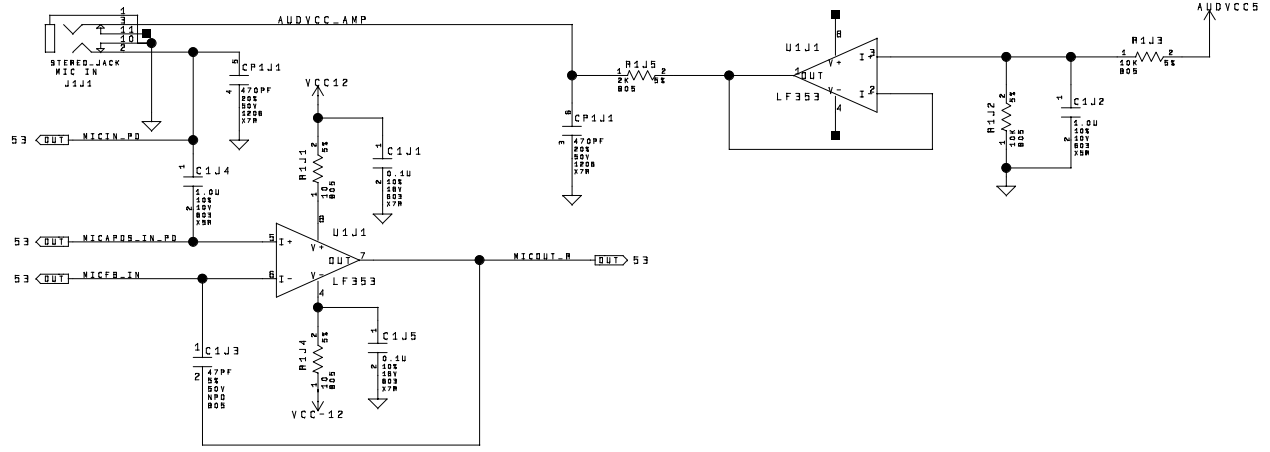


AUDIO NET

ROOM=AUD_CODEC

TITLE:		Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 3-9-2000 14:41	51 OF 53

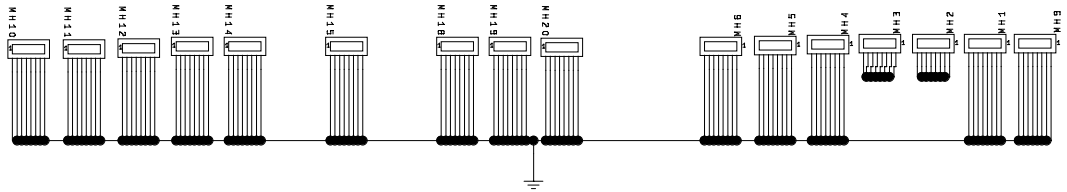




ROOM=BACK_PANEL

AUDIO LINE IN / LINE OUT / MIC IN

TITLE:	Rev: A
intel Embedded Intel Architecture	DRAWN BY: TL
	PROJECT:
LAST REVISED: 3-9-2000 14:41	52 OF 53



PCB MOUNTING HOLES

TITLE:		Rev: A
intel® Embedded Intel Architecture	DRAWN BY: TL	PROJECT:
	LAST REVISED: 2-4-2000 9:34	53 OF 53